Service Guide

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For Safety information, Warranties, and Regulatory information, see the pages at the end of the book.

Agilent Technologies 16760A Logic Analyzer

The Agilent 16760A Logic Analyzer—At a Glance

The Agilent Technologies 16760A is a 1500 Mb/s state/800-MHz timing logic analyzer modules for the Agilent Technologies 16700-series logic analysis system. The 16760A offers high performance measurement capability.

Features

Some of the main features of the 16760A are as follows:

- 32 data channels
- 2 clock/data channels
- 128Mb memory depth per channel
- 1500-MHz maximum state acquisition speed
- 800-MHz maximum timing acquisition speed
- Expandable to 170 channels

Service Strategy

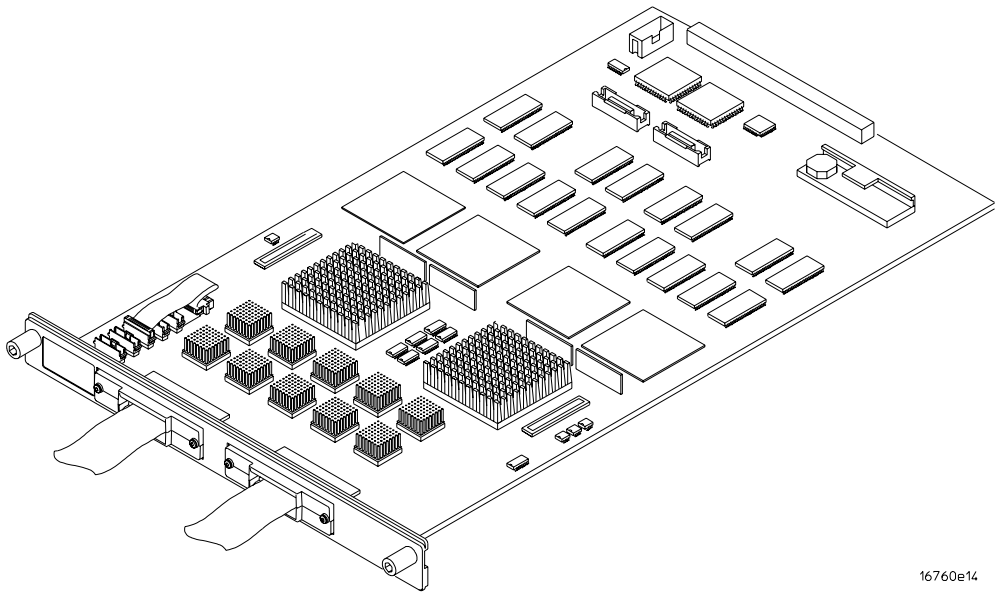
The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the 16760A state and timing analyzer module.

The modules can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

Application

This service guide applies to a 16760A module installed in the 16700-series logic analysis system mainframes.

The 16760A uses operating system version A.02.20.00 or higher. Agilent Technologies 16700-series mainframes with serial number prefix lower than US4111 are factory-installed with older operating system versions. If your mainframe operating system is older than the required version, contact your Agilent Technologies Service Center for newer software. Refer to Mainframe and Operating system on page 10 for more information.



The 16760A Logic Analyzer

In This Book

This book is the service guide for the 16760A 1500-Mb/s state/800-MHz timing logic analyzer modules. Place this service guide in the 3-ring binder supplied with your *Agilent Technologies 16700-Series Logic Analysis System Service Manual*.

This service guide has eight chapters.

Chapter 1 contains information about the module and includes accessories for the module, specifications and characteristics of the module, and a list of the equipment required for servicing the module.

Chapter 2 tells how to prepare the module for use.

Chapter 3 gives instructions on how to test the performance of the module.

Chapter 4 contains calibration instructions for the module.

Chapter 5 contains self-tests and flowcharts for troubleshooting the module.

Chapter 6 tells how to replace the module and assemblies of the module and how to return them to Agilent Technologies.

Chapter 7 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8 explains how the analyzer works and what the self-tests are checking.

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1

General Information

This chapter lists the accessories, the specifications and characteristics, and the recommended test equipment.

Accessories

One or more of the following accessories, not supplied, are required to operate the 16760A logic analyzer. Other accessories are listed in chapter 7 “Replacable Parts.”

Accessories	Agilent Part Number
100-pin single-ended probe	E5378A (available as 16760A #010)
100-pin differential probe	E5379A (available as 16760A #011)
38-pin single-ended probe	E5380A (available as 16760A #012)

Mainframe and Operating System

The 16760A logic analyzer requires an Agilent Technologies 16700-series logic analysis system with operating system version A.02.20.00 or higher. However, the specifications apply to operating system version A.02.50.00 or higher. The mainframe operating system must be upgraded to version A.02.50.00 before attempting the performance verification procedure in chapter 3. Request a software upgrade at http://software.cos.agilent.com/16700 or by contacting your nearest Agilent Technologies Customer Support Center. Agilent Technologies 16700-series mainframes with serial number prefix lower than US4148 are factory-installed with operating system versions older than A.02.50.00.

NOTE: Earlier versions of the 16700A/01A/02A mainframe contained only two cooling fans and might not provide adequate cooling to ensure reliable performance. If the first six digits of the 16700A/02A serial number (located on the back of the instrument) are US3849 or higher, or the first six digits of the 16701A are US3902 or higher, the instrument is a three-fan model, and there is sufficient cooling.

Specifications

The specifications are the performance standards against which the product is tested.

Threshold Accuracy	±(30 mV + 1.0% of threshold setting)
1500 Mb/s State Acquisition Mode:	
Maximum State Clock Rate	1500 MHz
Minimum Master-to-Master Clock Time*	666 ps
Setup/Hold Time (multiple clock edge)*	+3.0/-2.0 ns through -2.0/+3.0 ns
800 Mb/s State Acquisition Mode:	
Maximum State Clock Speed	800 MHz
Minimum Master-to-Master Clock Time*	1.25 ns
Setup/Hold Time (single clock edge)*	+3.0/-2.0 ns through -2.0/+3.0 ns
Setup/Hold Time (multiple clock edge)	+3.0/-2.0 ns through -2.0/+3.0 ns
400 Mb/s State Acquisition Mode:	
Maximum State Clock Speed	400 MHz
Minimum Master-to-Master Clock Time*	2.5 ns
Setup/Hold Time (single clock edge)*	+4.5/-2.0 ns through -2.0/+4.5 ns
Setup/Hold Time (multiple clock edge)*	+5.0/-2.0 ns through -1.5/+4.5 ns
200 Mb/s State Acquisition Mode:	
Maximum State Clock Speed	200 MHz
Minimum Master-to-Master Clock Time*	5.0 ns
Setup/Hold Time (single clock edge)*	+4.5/-2.0 ns though -2.0/+4.5 ns
Setup/Hold Time (multiple clock edge)*	+5.0/-2.0 ns through -1.5/+4.5 ns

*Specified for an input signal ≤ 800 mV peak-to-peak voltage swing 1V/ns slew rate, and using an Agilent E5378A probe.

Characteristics

The characteristics are not specifications, but are included as additional information.

	Full Channel	Half Channel
Maximum State Clock Rate	800 MHz	1500 MHz
Maximum Conventional Timing Rate	400 MHz	800 MHz
Channel Count per Card	34	17
Channel Count per Five-Card Module	170	85
Memory Depth	64M	128M

Environmental Characteristics

Probes

Maximum Input Voltage	± 40 V, CAT I, CAT I = Category I, secondary power line isolated circuits.

Auxiliary Power

Power Through Cables	1/3 amp at 5 V maximum per cable.

Operating Environment

Temperature	Instrument, 0 °C to 55 °C (+32 °F to 131 °F). Probe lead sets and cables, 0 °C to 65 °C (+32 °F to 149 °F).
Humidity	Instrument, probe lead sets, and cables, up to 95% relative humidity at +40 °C (+122 °F).
Altitude	To 4600 m (15,000 ft).
Vibration	Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈0.3 g (rms). Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis. Operating power supplied by mainframe. Indoor use only. Pollution Degree 2.

Recommended Test Equipment

Equipment Required

Equipment	Critical Specifications	Recommended HP/ Agilent Model/Part	Use*
Stimulus Board	no substitute	16760-60001	P,T
Pulse Generator	750 MHz, 1.0 ns pulse width, < 600 ps rise time	8133A Option 003	P,T
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A mainframe with 54751A plug-in module	P
20:1 Probes (Qty 2)		54006A	
SMA Coax Cable (Qty 5)	≥ 18 GHz bandwidth	8120-4948	P
BNC Coax Cable	BNC (m-m), > 2 GHz bandwidth	8120-1840	P
Adapter	SMA(m)-BNC(f)	1250-1200	P

P = Performance Tests, T = Troubleshooting

**Instructions for making these test connectors are in chapter 3, "Testing Performance."

2

Preparing for Use

This chapter gives you instructions for preparing the logic analyzer module for use.

Power Requirements

All power supplies required for operating the logic analyzer are supplied through the backplane connector in the mainframe.

Operating Environment

The operating environment is listed in chapter 1. Note the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer module will operate at all specifications within the temperature and humidity range given in chapter 1. However, reliability is enhanced when operating the module within the following ranges:

Temperature: +20 °C to +35 °C (+68 °F to +95 °F)

Humidity: 20% to 80% non-condensing

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40 °C to +75 °C (-40 °F to +167 °F)
- Humidity: Up to 90% at 65 °C
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the module from temperature extremes which cause condensation on the instrument.

To inspect the module

1 Inspect the shipping container for damage.

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2 Check the supplied accessories.

Accessories supplied with the module are listed in chapter 1, "Accessories Supplied."

3 Inspect the product for physical damage.

Check the module and the supplied accessories for obvious physical or

mechanical defects. If you find any defects, contact your nearest Agilent Technologies Sales Office. Arrangements for repair or replacement are made, at Agilent Technologies' option, without waiting for a claim settlement.

To prepare the mainframe

CAUTION: Turn off the mainframe power before removing, replacing, or installing the module.

CAUTION: Electrostatic discharge can damage electronic components. Use grounded wrist-straps and mats when performing any service to this module.

1 Remove power from the instrument.

   a Exit all logic analysis sessions. In the session manager, select Shutdown.

   b At the query, select Power Down.

   c When the "OK to power down" message appears, turn the instrument off.

   d Disconnect the power cord.

   e Disconnect any input or output connections.

2 Plan your module configuration.

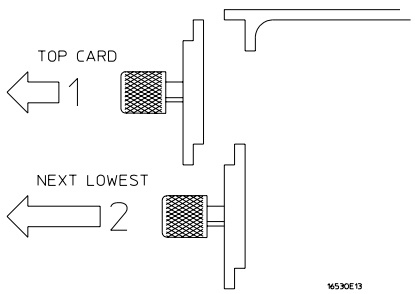
   If you are installing a one-card module, use any available slot in the mainframe.

   If you are installing a multi-card module, use adjacent slots in the mainframe.

3 Loosen the thumb screws.

   Cards or filler panels below the slots intended for installation do not have to be removed.

   Starting from the top, loosen the thumb screws on filler panels and cards that need to be moved.



4 Starting from the top, pull the cards and filler panels that need to be moved halfway out.

CAUTION: All multi-card modules will be cabled together. Pull these cards out together.

5 Remove the cards and filler panels.

Remove the cards or filler panels that are in the slots intended for the module installation. Push all other cards into the card cage, but not completely in. This is to get them out of the way for installing the module.

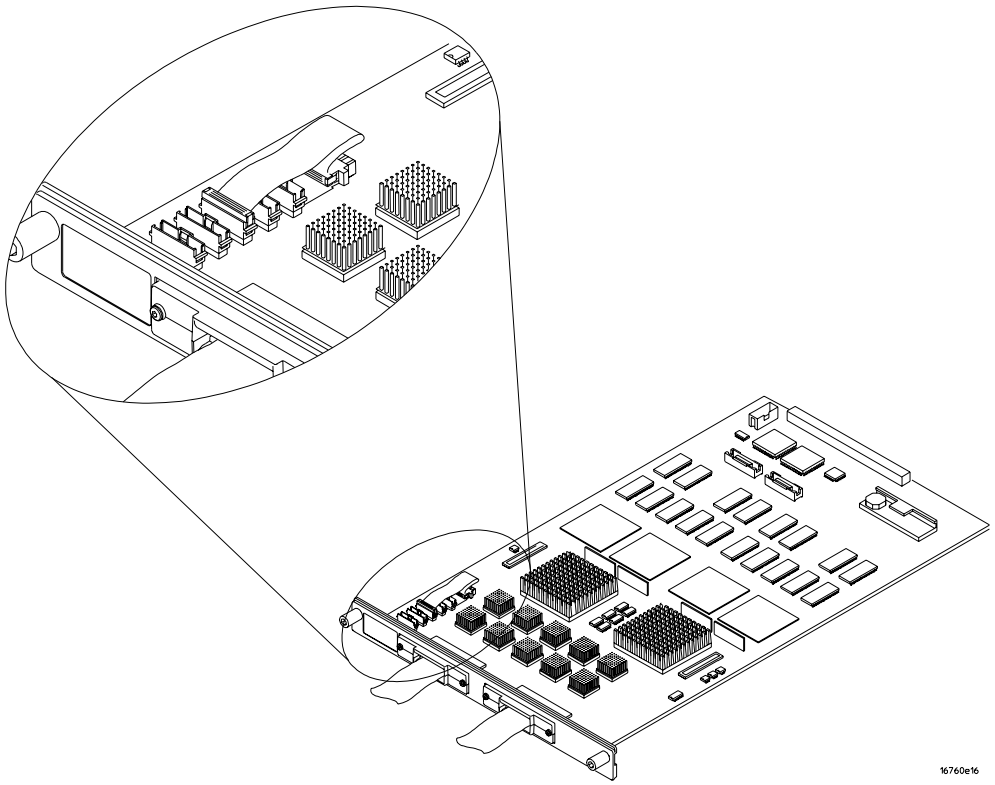
Some modules for the Logic Analysis System require an operational accuracy calibration if you move them to a different slot. For calibration information, refer to the manuals for the individual modules.

To configure a one-card module

- When shipped separately, the module is configured as a one-card module. The cables should be connected as shown in the figure.
- To configure a multicard module into one-card modules, remove the cables connecting the cards. Then connect the free end of the 2x10 cable to the connector labeled "Master" (J6) on each card (see figure below).

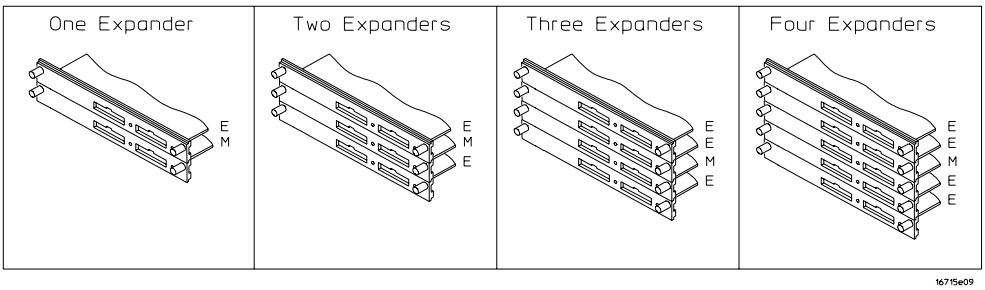
CAUTION: If you pull on the flexible ribbon part of the 2x10 cable, you might damage the cable assembly. Using your thumb and finger, grasp the ends of the cable connector. Apply pressure to the ends of the cable connector to disengage the metal locking tabs of the connector from the cable socket on the board. Then pull the connector from the cable socket.

NOTE: Save unused cables for future configurations.



To configure a multi-card module

1 Plan the configuration. Multicard modules can only be connected as shown in the illustration. Select the card that will be the master card, and set the remaining cards aside.



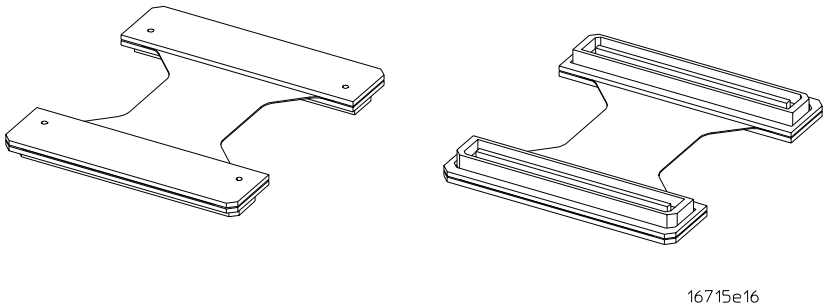
2 Obtain two 2x40 cables from the accessory pouch for every expander card being configured.

One Expander: Two 2x40 cables

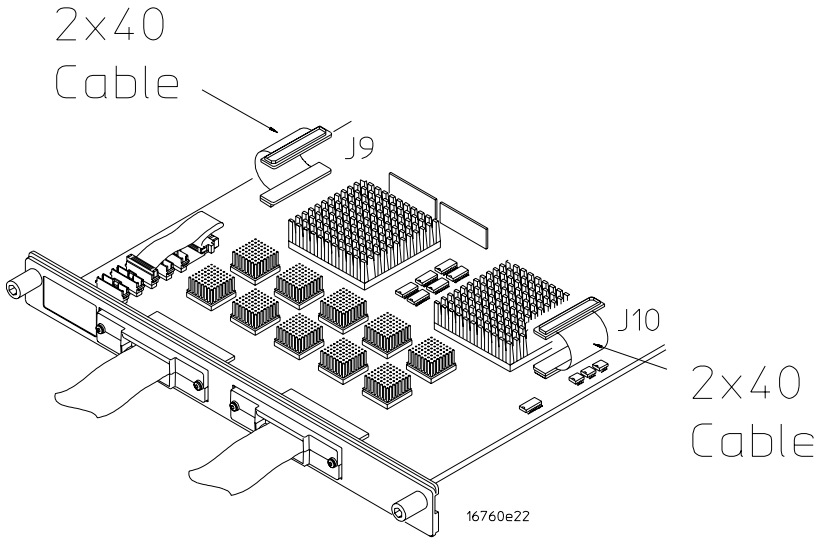
Two Expanders: Four 2x40 cables

Three Expanders: Six 2x40 cables

Four Expanders: Eight 2x40 cables.

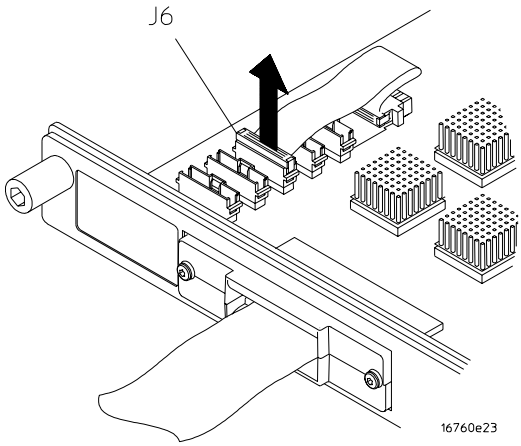


3 Connect a 2x40 cable to J9 and to J10 of each card in the multicard configuration.

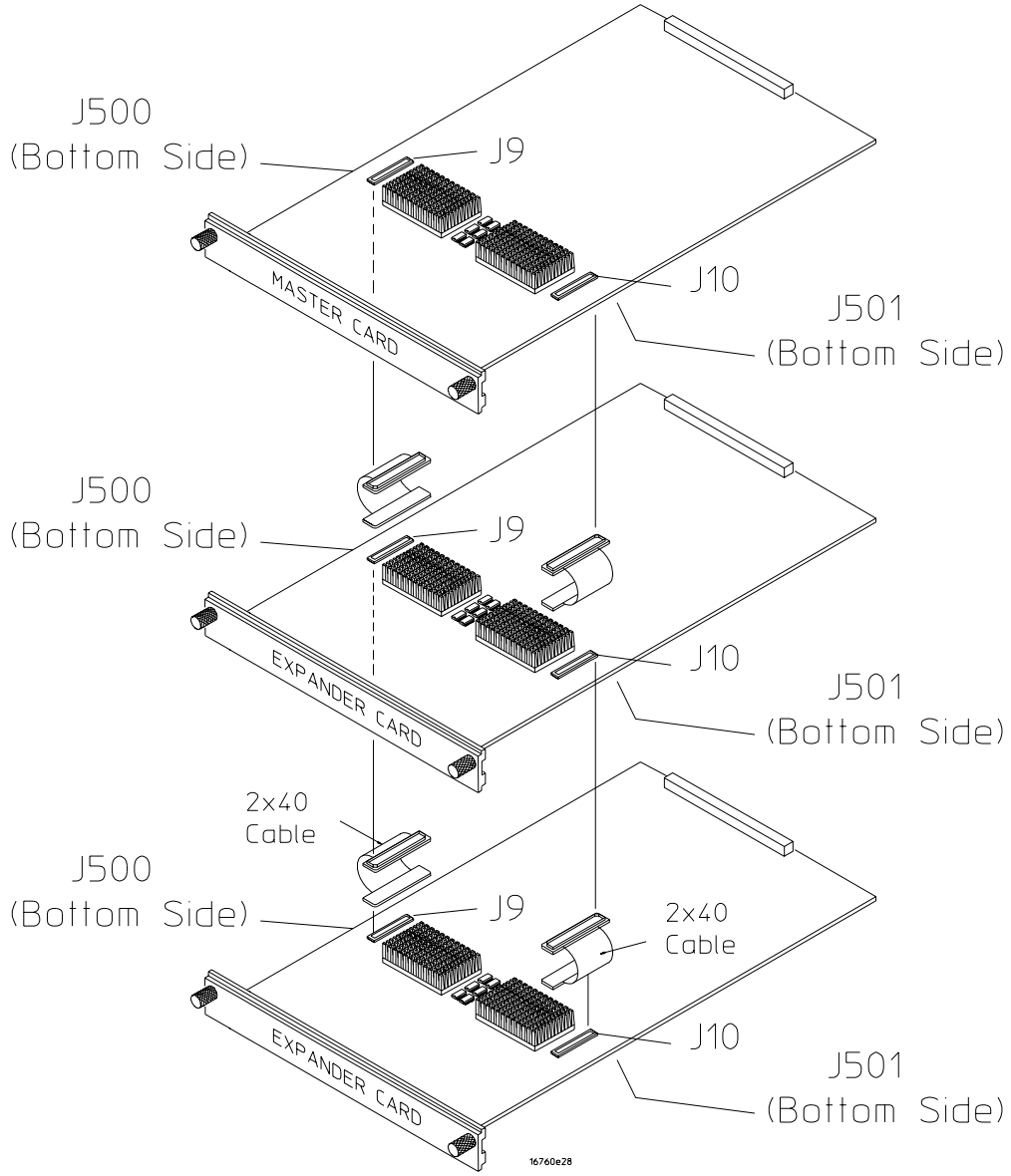


4 On the expander cards, disconnect the end of the 2x10 cable that is plugged into the connector labeled "Master."

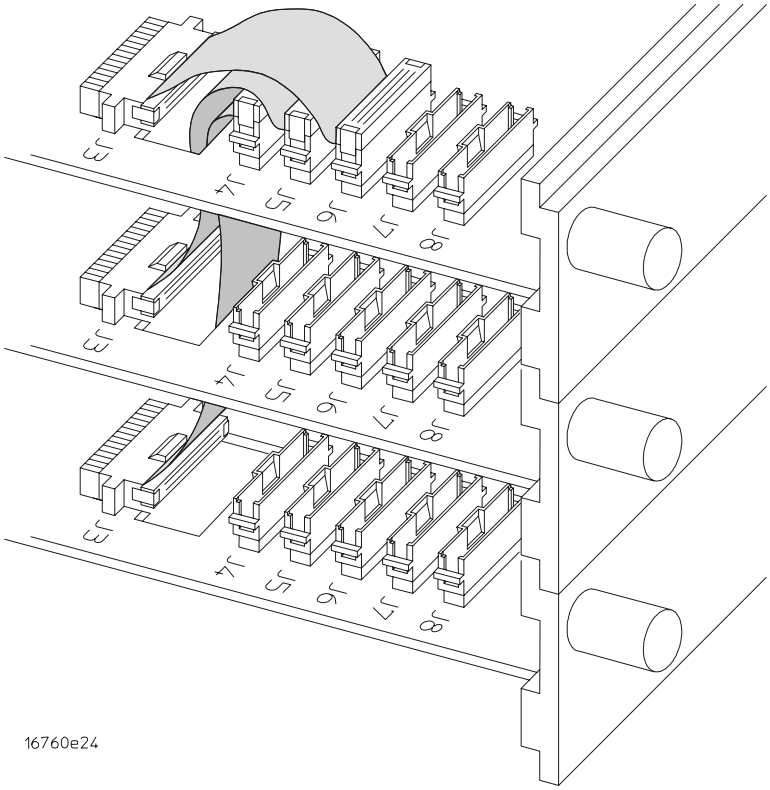
CAUTION: If you pull on the flexible ribbon part of the 2x10 cable, you might damage the cable assembly. Using your thumb and finger, grasp the ends of the cable connector. Apply pressure to the ends of the cable connector to disengage the metal locking tabs of the connector from the cable socket on the board. Then pull the connector from the cable socket.



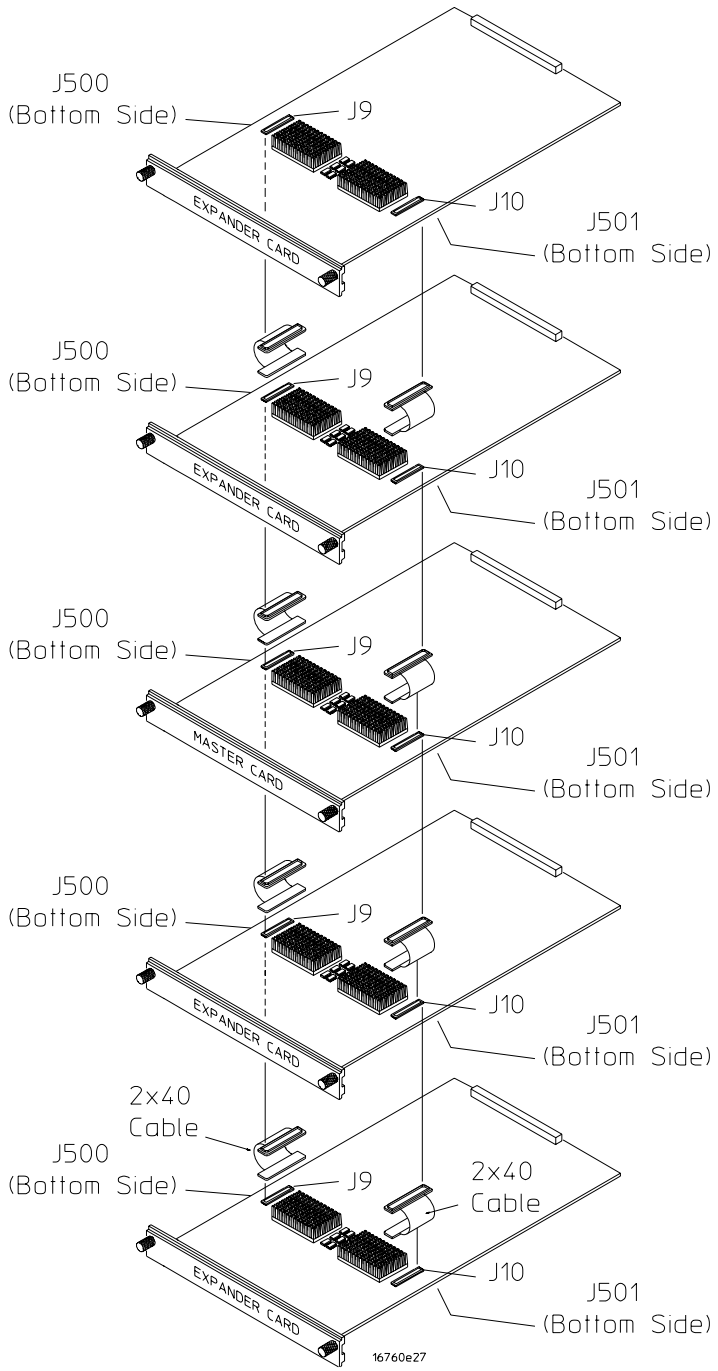
5 Begin stacking the cards together according to the drawing under step 1. While stacking, connect the free end of the 2x40 cable on the lower card J9 to J500 of the upper card, on the underside of the card. Connect the free end of the 2x40 cable on the lower card J10 to J501 of the upper card, on the underside of the card



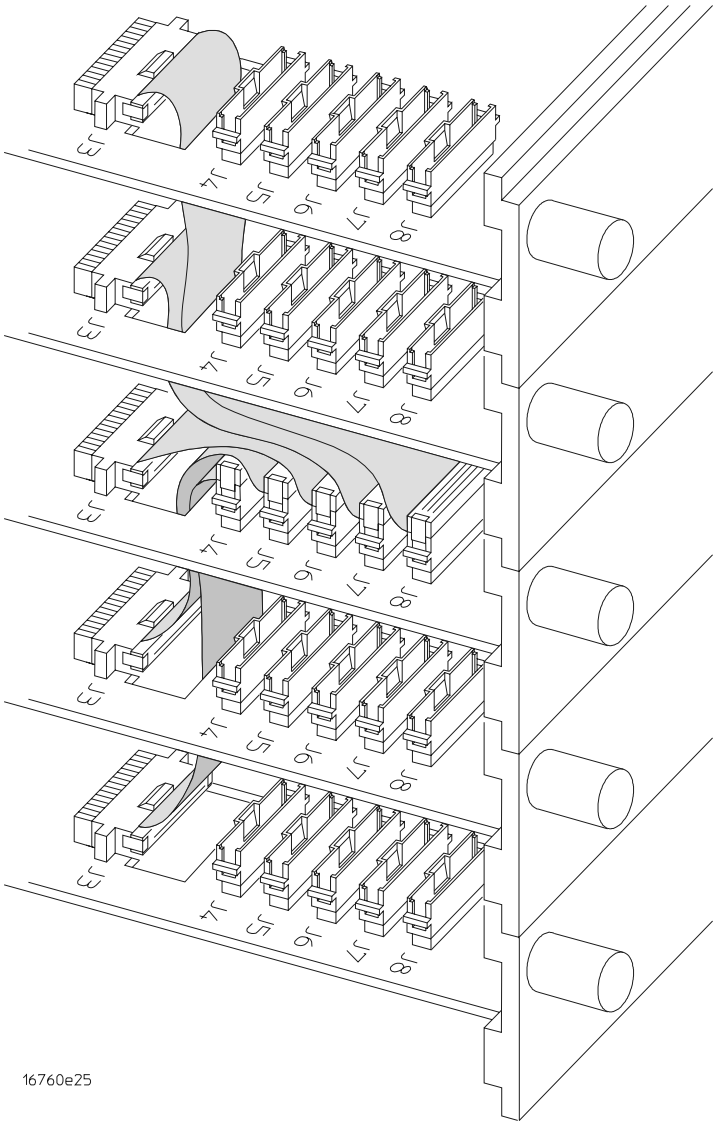
6 Feed the free end of the 2x10 cables of the lower expander cards through the access holes to the master card. Plug the 2x10 cables into J4 (bottom-most expander in a five-card configuration) and J5 (expander that is next to the master card) on the master card.



7 Stack the remaining expander boards on top of the master board. While stacking, connect the free end of the 2x40 cables on the lower card J10 and J9 to the upper card J501 and J500.



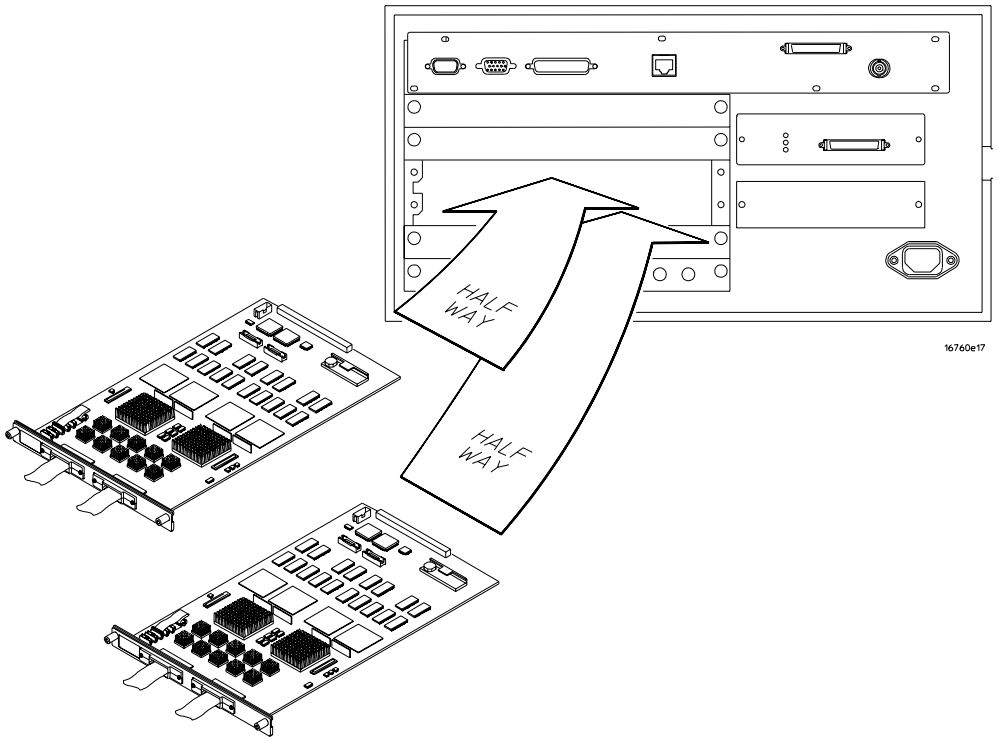
8 Feed the free end of the 2x10 cables of the expander cards through the access holes to the master card. Plug the 2x10 cables into J7 (expander that is next to the master card) and J8 (top-most expander in a four- or five-card configuration) on the master card.



To install the module

1 Slide the cards above the slots for the module about halfway out of the mainframe.

2 With the probe cables facing away from the instrument, slide the module approximately halfway into the mainframe.



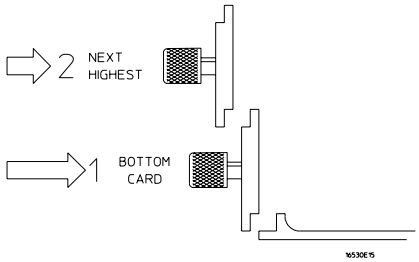
3 Slide the complete module into the mainframe, but not completely in.

Each card in the instrument is firmly seated and tightened one at a time in step 5.

4 Position all cards and filler panels so that the endplates overlap.

5 Seat the cards and tighten the thumbscrews.

Starting with the bottom card, firmly seat the cards into the backplane connector of the mainframe. Keep applying pressure to the center of the card endplate while tightening the thumbscrews finger-tight. Repeat this for all cards and filler panels starting at the bottom and moving to the top.



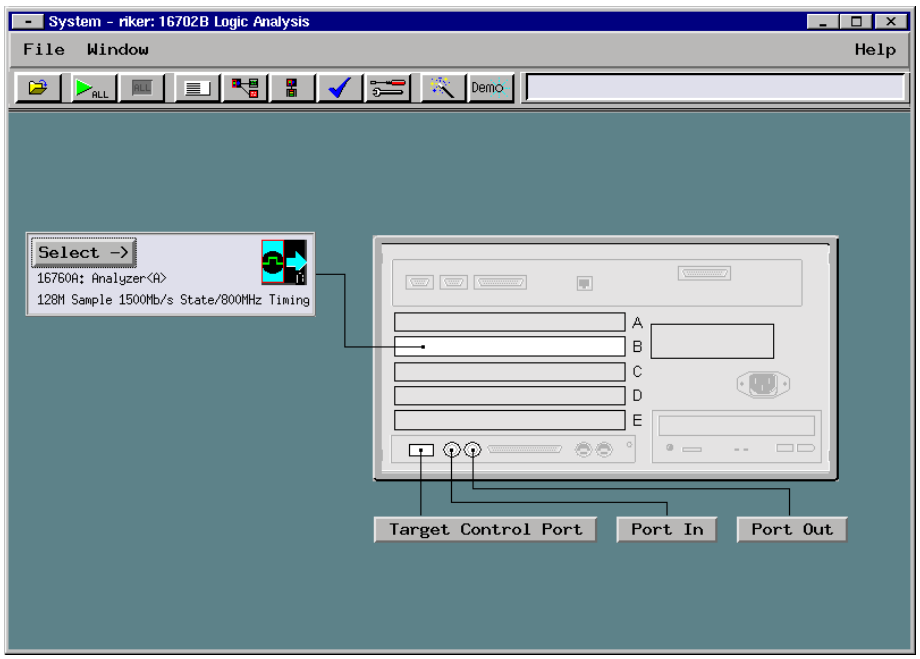
CAUTION: Correct air circulation keeps the instrument from overheating. For correct air circulation, filler panels must be installed in all unused card slots. Keep any extra filler panels for future use.

To turn on the system

1 Connect the power cable to the mainframe.

2 Turn on the instrument power switch.

When you turn on the instrument power switch, the instrument performs powerup tests that check mainframe circuitry. After the powerup tests are complete, the screen will look similar to the sample screen below.



To test the module

The logic analyzer module does not require an operational accuracy calibration or adjustment. After installing the module, you can test and use the module.

- If you require a test to verify the specifications, start at the beginning of chapter 3, "Testing Performance."
- If you require a test to initially accept the operation, perform the self-tests in chapter 3.
- If the module does not operate correctly, go to the beginning of chapter 5, "Troubleshooting."

To clean the module

- With the mainframe turned off and unplugged, use mild detergent and water to clean the rear panel.
- Do not attempt to clean the module circuit board.

3

Testing Performance

This chapter tells you how to test the performance of the logic analyzer against the specifications listed in chapter 1.

To ensure the logic analyzer is operating as specified, software tests (self-tests) and manual performance tests are done. The logic analyzer is considered performance-verified if all of the software tests and manual performance tests have passed. The procedures in this chapter indicate what constitutes a “Pass” status for each of the tests.

Test Strategy

This chapter shows the module being tested in an Agilent Technologies 16700B-series mainframe. For a complete test, start at the beginning with the software tests and continue through to the end of the chapter. For an individual test, follow the procedure in the test.

One-card Module. To perform a complete test on a one-card module, start at the beginning of the chapter and follow each procedure.

Multi-card Module. To perform a complete test on a multi-card module, perform the self-tests with the cards connected. Then, remove the multi-card module from the mainframe and configure each card as a one-card module. Install the one-card modules into the mainframe and perform the one-card manual performance verification tests on each card. When the tests are complete, remove the one-card modules, reconfigure them into a multi-card module, reinstall it into the mainframe and perform the final multi-card test. For removal instructions, see Chapter 6, “Replacing Assemblies.” For installation and configuration instructions, see Chapter 2, “Preparing for Use.”

Test Interval

Test the performance of the module against specifications at two-year intervals.

Test Record Description

A performance test record for recording the results of each procedure is located at the end of this chapter. Use the performance test record to gauge the performance of the module over time.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number.

Instrument Warm-Up

Before testing the performance of the module, warm-up the instrument and the test equipment for 30 minutes.

To Perform the Self-tests

There are two types of self-tests: self-tests that automatically run at power-up, and self-tests that you select on the screen. The self-tests verify the correct operation of the logic analysis system. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analysis system, run the self-tests all at once.

Perform the power-up tests

The logic analysis system automatically performs power-up tests when you apply power to the instrument. Any errors are reported in the boot dialogue. Serious errors will interrupt the boot process.

The power-up tests are designed to complement the instrument on-line Self Tests. Tests that are performed during power-up are not repeated in the Self Tests.

The monitor, keyboard and mouse must be connected to the mainframe to observe the results of the power-up tests.

1. Disconnect all inputs and exit all logic analysis sessions.

   In the Session Manager, select **Shutdown**. In the window, select **Powerdown**.

2. When the "OK to power down" message appears, turn off the power switch.

3. After a few seconds, turn the power switch back on. Observe the boot dialogue for the following:

   - ensure all of the installed memory is recognized
   - any error messages
   - interrupt of the boot process with or without error message

   A complete transcript of the boot dialogue is in the *Agilent Technologies 16700B-Series Logic Analysis System Service Guide*, Chapter 8, "Theory of Operation".

4. During initialization, check for any failures.

   If an error or an interrupt occurs, refer to the *Agilent Technologies 16700B-Series Logic Analysis System Service Guide*, Chapter 5, "Troubleshooting".

Perform the self-tests

The self-tests verify the correct operation of the logic analysis system and the installed 16760A module. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analysis system, run the self-tests all at once.

1 Launch the Self-Tests.

a In the System window, click on System Admin.

b Under the Admin tab, click on Self-Test. . .

c In the query pop-up, select Yes to exit the current session.

The Self-Test closes down the current session because the test algorithms leave the system in an unknown state. Re-launching a session at the end of the tests will ensure the system is properly initialized.

2 In the Self-Test window select Test All.

When the tests are finished, the Status will change to TEST passed or TEST failed. You can find detailed information about the test results in the Status Message field of the Self-Test window.

The System CPU Board test returns Untested because the CPU tests require user action. To test the CPU Board, select CPU Board, then select each test individually.

3 Select Quit to exit the Test menu.

4 In the Session Manager, select Start Session to re-launch a logic analysis session.

To Set up the Test Equipment and the Analyzer

Before testing the specifications of the 16760A logic analyzer, the test equipment and the logic analysis system must be set up and configured.

These instructions include detailed steps for initially setting up the required test equipment and the logic analysis system. Before performing any or all of the following tests in this chapter, the following steps must be followed.

NOTE: Multi-card modules must be separated into single-card modules.

Equipment Required

Equipment	Critical Specifications	Recommended HP/Agilent Model/Part
Pulse Generator	750 MHz, 1.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Stimulus Board	no substitute	16760-60001
SMA Coax Cable (Qty 3)	> 18 GHz Bandwidth	8120-4948

Set up the equipment

1. Turn on the required test equipment listed in the table above. Let them warm up for 30 minutes before beginning any test.
2. Turn on the logic analysis system.
   - **a** Connect the keyboard and monitor to the rear panel of the logic analysis system mainframe (16700B only).
   - **b** Connect the mouse to the rear panel of the mainframe.
   - **c** Plug in the power cord to the power connector on the rear panel of the mainframe.
   - **d** Turn on the main power switch on the mainframe front panel.
3. Set up the logic analysis system.
   - **a** Open the Session Manager window and select “Start Session.”
   - **b** In the Logic Analysis System window, select the module icon, then select Setup and Trigger. A Setup and Trigger window will appear.

4 Set up the pulse generator according to the following tab.

Timebase	**Channel 2**	**Trigger**	**Channel 1**
Mode: Int	Mode: Square	Divide: Divide ÷ 2	Mode: Square
Period: 5.000 ns	Divide Square ÷ 1	Ampl: 0.50 V	Delay: 0 ps
	Ampl: 0.80 V		Ampl: 0.80 V
	Offs: 2.00 V		Offs: 2.00 V
	COMP: Disabled		COMP: Disabled
	(LED Off)		(LED Off)

5 Set up the oscilloscope.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift]** ΔTime
Averaging On: # of averages: 16	Graticule graphs: 2	Level: 0.0 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define** ΔTime
External Scale Attenuation: 20.00:1	External Scale Attenuation: 20.00:1	Start edge: either
Scale: 200 mV/div	Scale: 200 mV/div	Edge number: 1
Offset: 1.000 V	Offset: 1.000 V	Edge threshold: middle
		Stop edge: either
		Edge number: 3
		Edge threshold: middle

c Using a SMA cable, connect the pulse generator trigger output to the oscilloscope trigger input.

Allow the logic analysis system to warm up for 30 minutes before beginning any of the following tests.

Connect the logic analyzer

1 Connect the pulse generator to the stimulus board.

a Using the SMA cable connect the pulse generator channel 2 OUTPUT to the stimulus board J6 input.

b Using an SMA cable, connect the pulse generator channel 1 OUTPUT to the stimulus board J7 input.

c Connect a power cord to the stimulus board power supply. Connect the stimulus board power supply output to the stimulus board power supply connector J82.

Do not turn on the stimulus board yet. The stimulus board in its quiescent state will be used to verify the threshold accuracy specification.

2 Set up the stimulus board.

a Configure the oscillator select switch S1 according to the following settings:

- S1 Off
- S2 Off
- S3 Off
- Ext

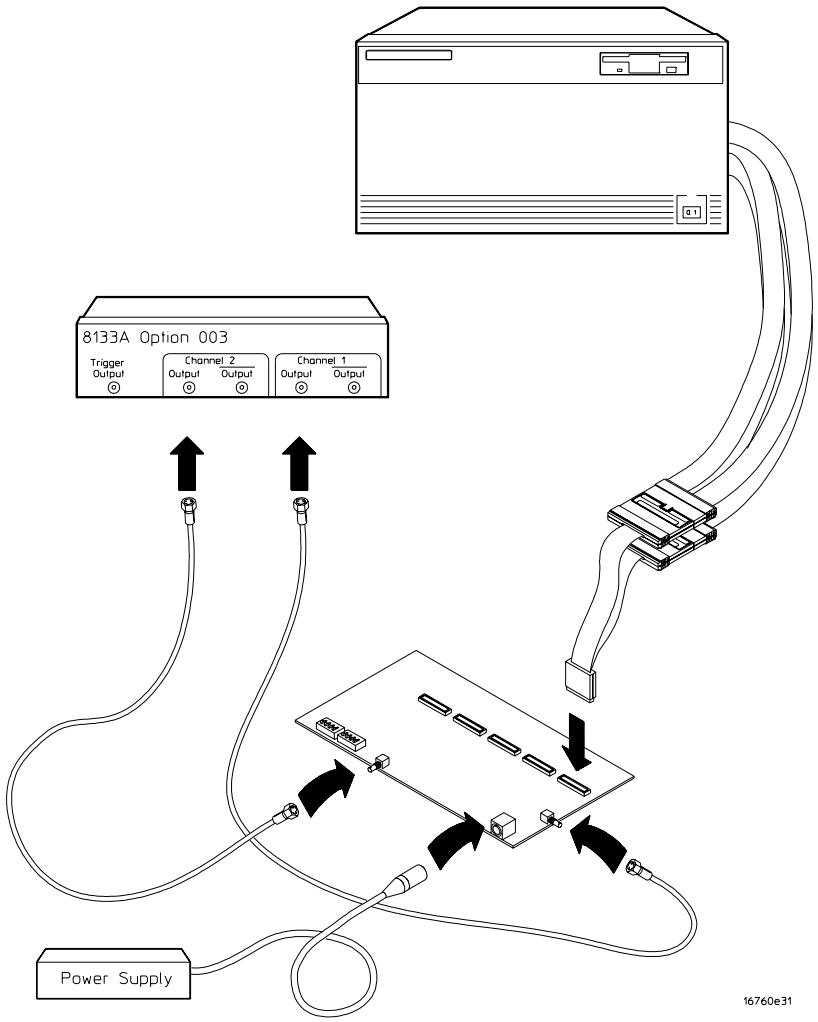
b Configure the data mode switch S4 according to the following settings.

- Even
- Toggle

3 Connect the logic analyzer to the stimulus board.

a Connect an E5378A 100-pin single-ended probe to the logic analyzer. connect the logic analyzer Pod 1 to the high density probe adapter output marker “Odd.” Connect logic analyzer Pod 2 to the high density probe adapter output marked “Even.”

b Connect the probe adapter input to stimulus board connector Pod 5.



To Test the Threshold Accuracy

Testing the threshold accuracy verifies the performance of the following specification:

- Clock and data channel threshold accuracy

Equipment Required

Equipment	Critical Specifications	Recommended HP/Agilent Model/Part
Pulse Generator		8133A Options 003
Stimulus Board	no substitute	16760-60001
SMA Coax Cable	> 18 GHz Bandwidth	8120-4948

Set up the equipment

If you have not already done so, do “Set up the equipment” on page 35.

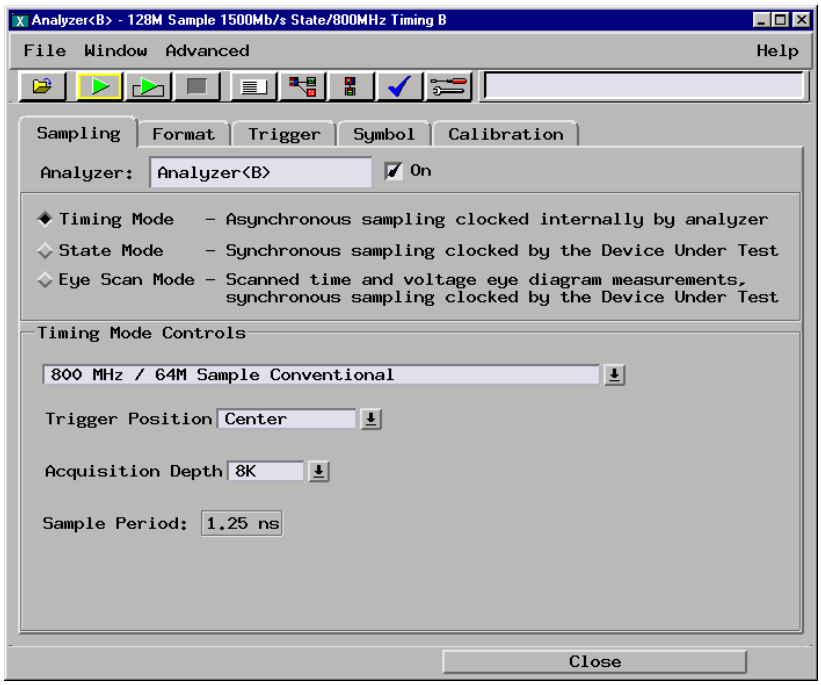
Set up the logic analyzer

1 Configure the Sampling tab.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select Timing Mode.

c Select the Acquisition Depth field, then select 8K.

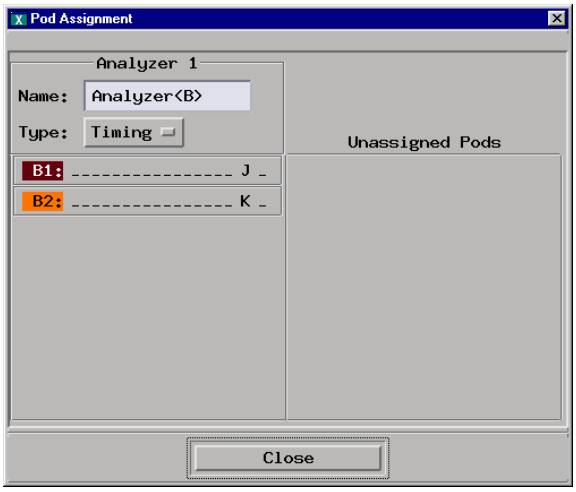


2 Configure the Format tab.

a In the logic analyzer Setup and Trigger window, select the Format tab.

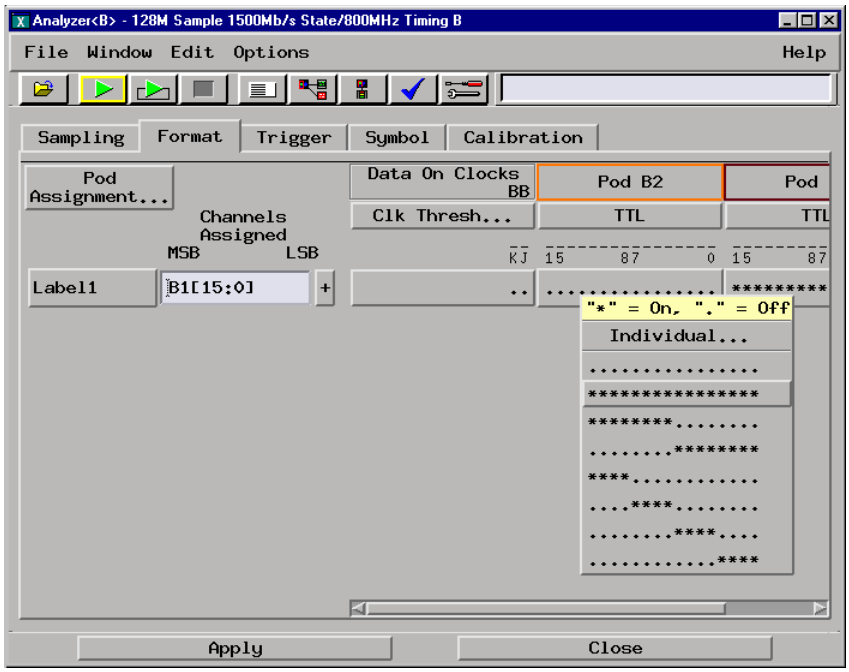
b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag the pods to the Analyzer 1 column.



d Select Close to close the pod assignment window.

e Under the Format tab, select the field showing the channel assignments for one of the pods being tested, then select "**********".



f Repeat step e for the remaining pod to be tested. All channels on pods 1 and 2 should now be assigned to Label1.

3 Open the Waveform window.

a In the Setup and Trigger window, select Window, then select Slot<n>: Analyzer<n> (where n is the slot the module under test is installed).

b At the pop-up menu, select Waveform. The Waveform window will appear.

Verify the 0V threshold accuracy

1 Initialize the threshold setting.

a In the Setup and Trigger window under the Sampling tab, select the threshold field under either pod. The Pod threshold window will appear.

b In the Pod threshold window, ensure Apply threshold settings to all pods is checked.

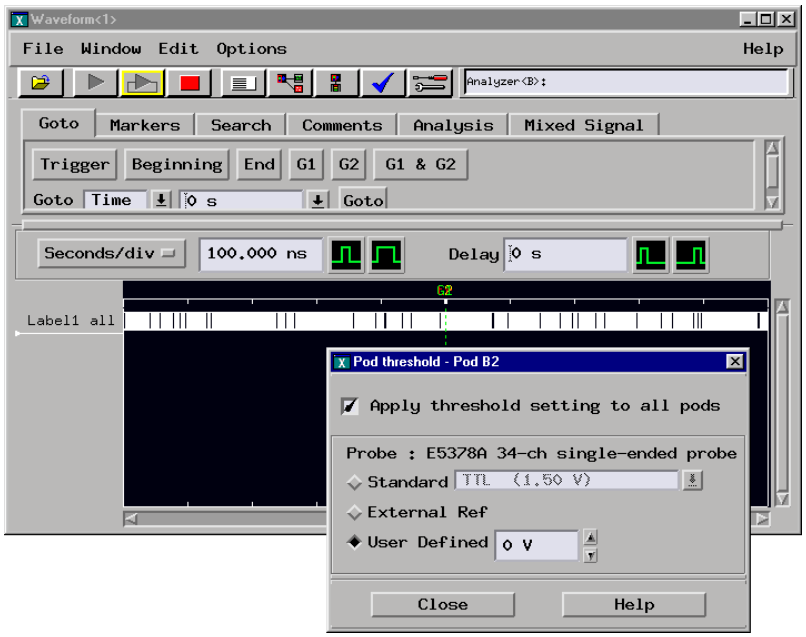
c In the Pod threshold window, select User Defined, then select the threshold voltage field. Enter 0V in the User Defined threshold voltage field.

NOTE: Leave the Pod threshold window open. You will be changing the threshold voltage value while performing the test.

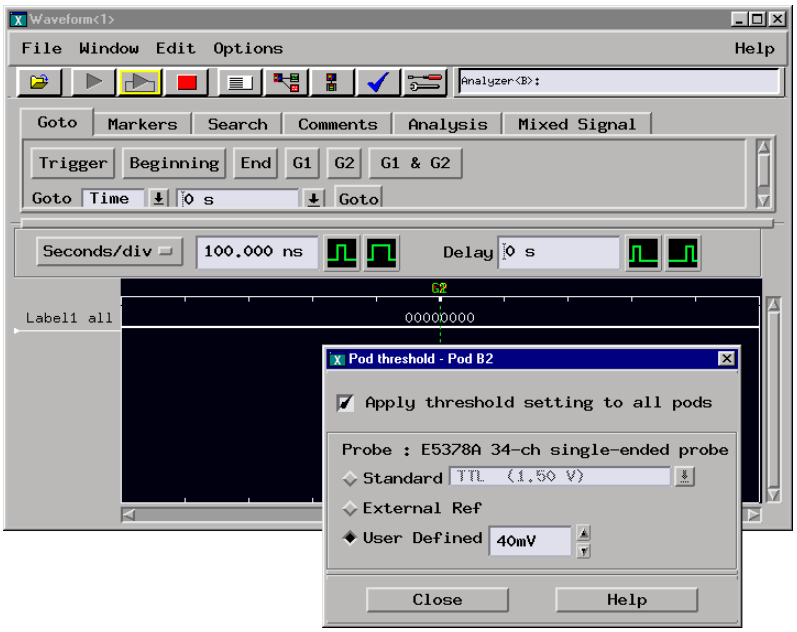
2 Verify the test data.

a In the Waveform window, select the Run-Repetitive icon. Activity should appear in the Label1 waveform.

b Using the mouse, move the Waveform window and the Pod threshold window so you can observe the Label1 waveform in the Waveform window while adjusting the threshold in the Pod threshold window.

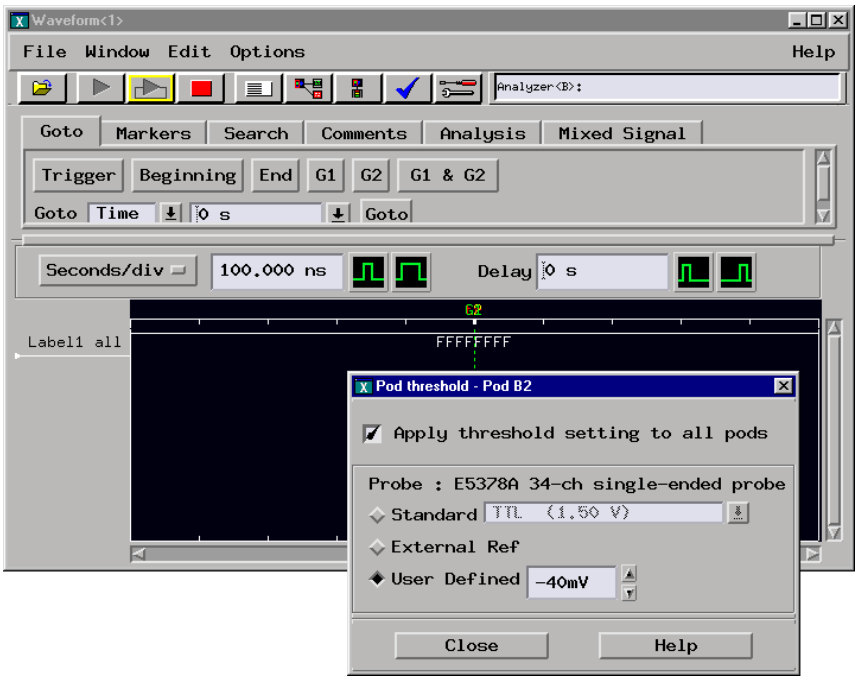


c Using the mouse, increase the threshold voltage by clicking on the up arrow next to the User Define threshold voltage field in the Pod threshold window until the Label1 waveform shows “00000000”. Allow a few seconds settling time between mouse clicks.



Enter the threshold voltage setting here: V_H = _____ mV.

d Using the mouse, decrease the threshold voltage by clicking on the down arrow next to the User Defined threshold voltage field in the Pod threshold window until the Label1 waveform shows “FFFFFFFF”. Allow a few seconds settling time between mouse clicks.



Enter the threshold setting here: V_L = _____ mV.

e Calculate the logic analyzer threshold voltage using the formula (observe signs):

$$V_{th} = \frac{V_H + V_L}{2} = \_\_\_\_\_ \text{ mV}$$

The V_{th} voltage should be between -30mV and 30mV. If the result is in this range, then record a Pass in the performance test record.

3 End the test.

a In the Waveform window, select the Stop icon to the stop the acquisition.

b In the Waveform window, select the [X] field in the upper right corner of the window to close the window.

c In the Pod threshold window, select Close to close the window.

d In the Setup and Trigger window, select the [X] field in the upper right corner of the window to close the window.

e In the Logic Analysis System window, select [X] field to close the window. At the query, select OK.

Ending and restarting the logic analysis session will reinitialize the system for the state mode tests.

To configure the analyzer for the state mode tests

Before testing the state mode specifications of the 16760A logic analyzer, the logic analysis system must be configured and stimulus board threshold characterized.

Equipment Required

Equipment	Critical Specifications	Recommended HP/Agilent Model/Part
Pulse Generator	750 MHz, 1.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Stimulus Board	no substitute	16760-60001
SMA Coax Cable (Qty 5)	> 18 GHz Bandwidth	8120-4948
20:1 probe (Qty 2)		54006A

Set up the equipment

If you have not already done so, do “Set up the equipment” on page 35.

Activate the stimulus board

1 Plug in the stimulus power supply into line power. The green LED DS1 should illuminate showing that the stimulus board is active.

CAUTION: The stimulus board gets warm to the touch under normal operation. Avoid prolonged physical contact with any part of the board while doing any of the performance tests.

2 On the stimulus board, press the Resynch VCO button.

Set up the logic analysis system

1 Set up the logic analysis system.

a Open the Session Manager window and select Start Session.

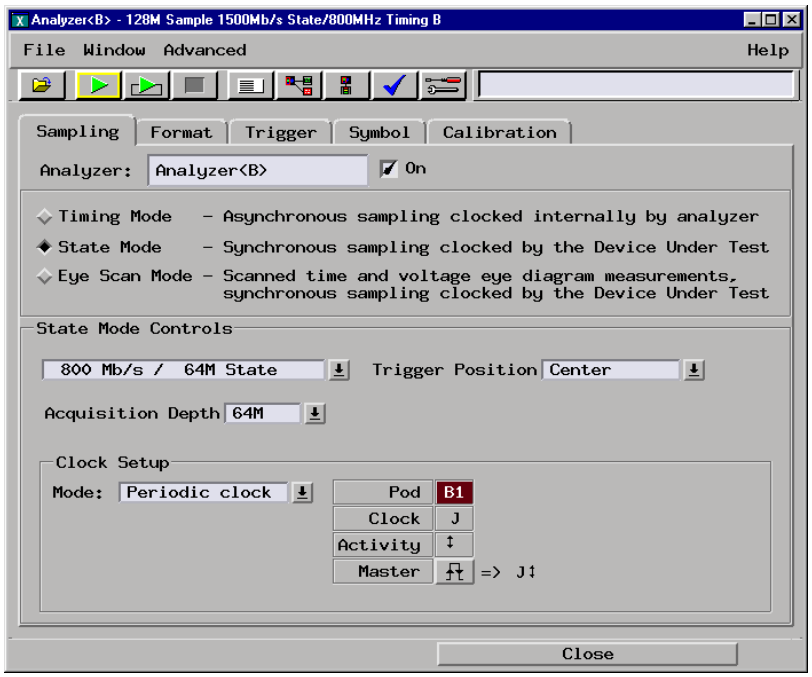
b In the Logic Analysis System window, select the module icon, then select Setup and Trigger. A Setup and Trigger window opens.

2 Configure the Sampling tab.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select State Mode.

c Select the clock edge field for J-clock, then select Both Edges.



3 Configure the Trigger settings.

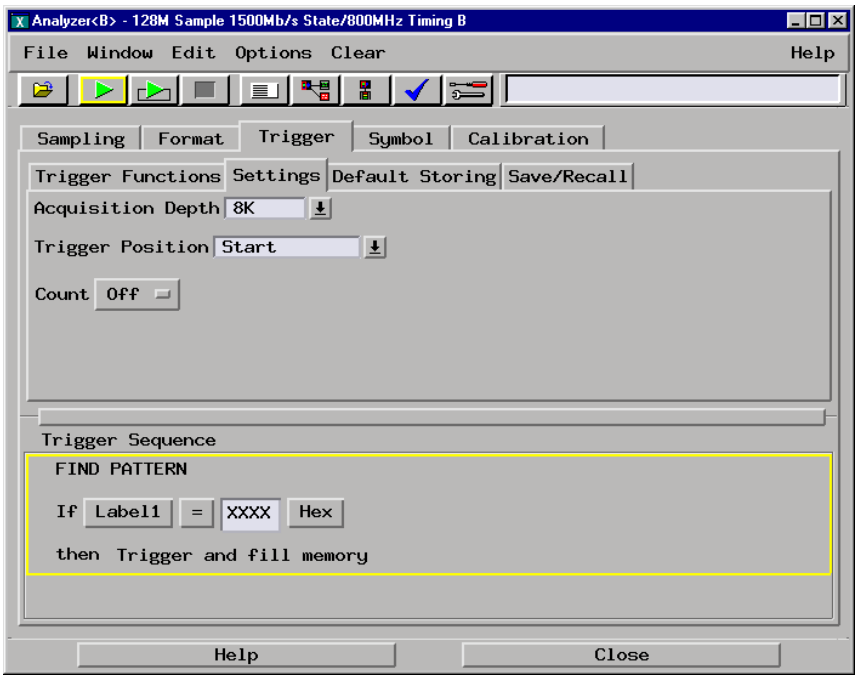
a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger tab, select the Settings tab.

c Select the Acquisition Depth field, then select 8K.

d Select the Trigger Position field, then select Start.

e Select the Count field, then select Off.

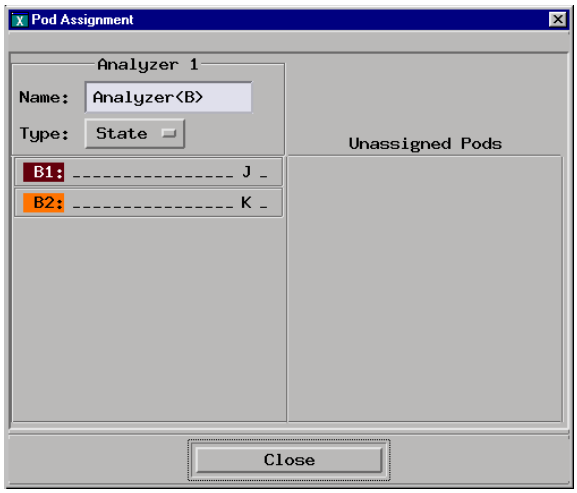


4 Configure the Format tab.

a In the logic analyzer Setup and Trigger window, select Format tab.

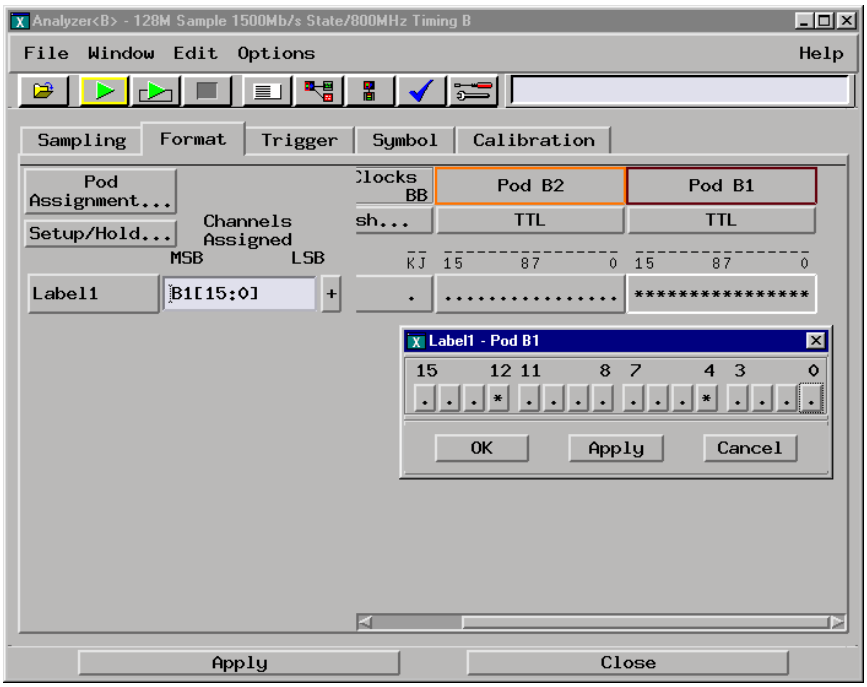
b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag the pods to the Analyzer 1 column.



d Select Close to close the Pod Assignment window.

e Under the Format tab, select the field showing the channel assignment for one of the pods being tested, then select Individual. Using the mouse, select the data channels to be tested (channels 12 and 4 of each pod). An asterisk (*) means that a channel is turned on.



f Select OK to close the channel assignment window.

g Repeat e and f for the remaining pods to be tested.

5 Configure the Listing window.

a In the Setup and Trigger window, select Window, then select Slot<n>: Analyzer<n> (where n is the slot the module under is installed). At the pop-up menu, select Listing. The Listing window will appear.

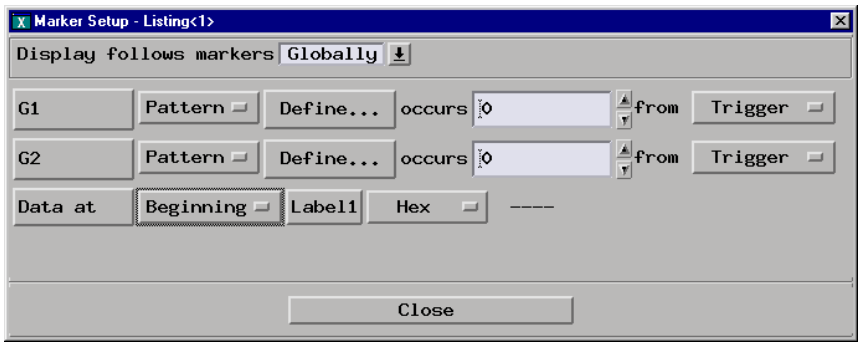
b In the Listing window, select the Markers tab.

c Select the G1: field and the Markers Setup window appears.

d Select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.

e Right-click on the Interval field and select Delete.

f Select the Trigger field associated with Data at and select Beginning.



NOTE: Leave the Marker Setup window open. You will be entering numeric values in the "occurs" field after acquiring the first run of test data.

6 Configure the Markers.

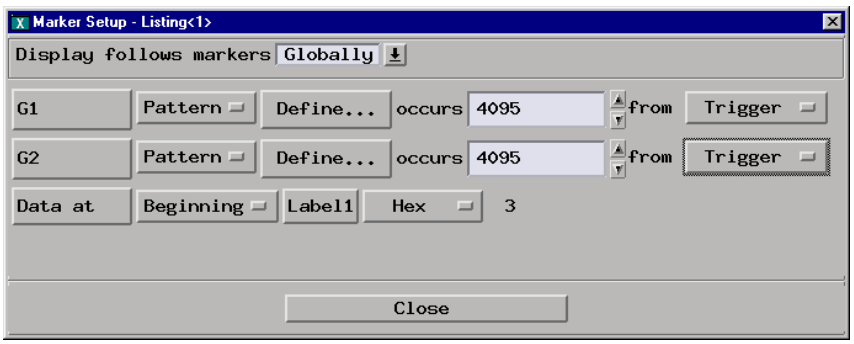
Do the following steps after acquiring the first run of test data.

a In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the pattern field, enter "C". Select Apply, then select Close.

b In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the pattern field, enter "3". Select Apply, then select Close.

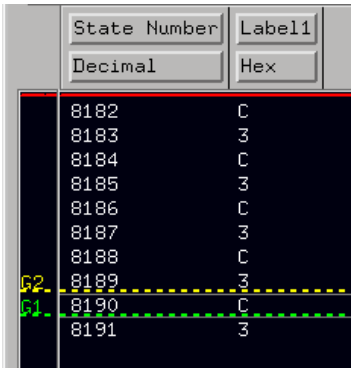
c In the Marker Setup window, select the 'occurs' value field that corresponds to marker G1. Enter 4095.

d In the Marker Setup window, select the 'occurs' value field that corresponds to marker G2. Enter 4095.



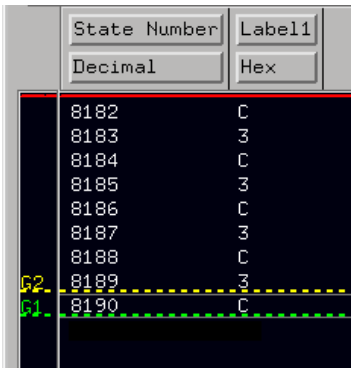
A PASS is determined by the markers counting the number of correct states. However, because the acquisition is prone to one prestore state, the Marker Setup window is configured to monitor the first state and the G2 marker is configured to count one less occurrence of the data "3".

With no prestore state, the Listing window will show:



The Data at field in the Marker Setup window will show C as the data in the first stored state, the trigger state.

With one prestore state, the Listing window will show:



The Data at field in the Marker Setup window will show 3 as the data in the first stored state, the prestore state.

Either of the above results passes the test.

Characterize the stimulus board output threshold

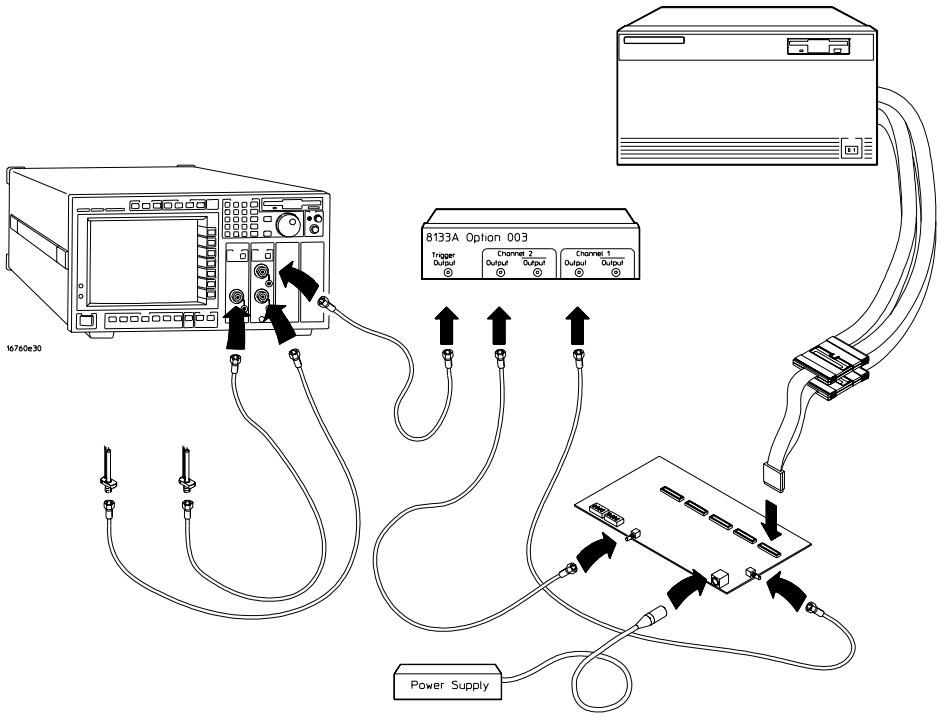
This procedure is only required the first time the stimulus board is used for calibration. After measuring the average voltage of the stimulus board signals, you will use it to configure both the logic analyzer threshold and the oscilloscope measure thresholds. Once you have measured the V avg, it can be used to configure the logic analyzer and oscilloscope thresholds for all future calibrations.

1 Set up the oscilloscope.

a Configure two 54006A probes with 950 **Ω** resistors.

b Connect one end of an SMA cable to the channel 1 input of the oscilloscope. Connect the free end of the SMA cable to one 54006A probe.

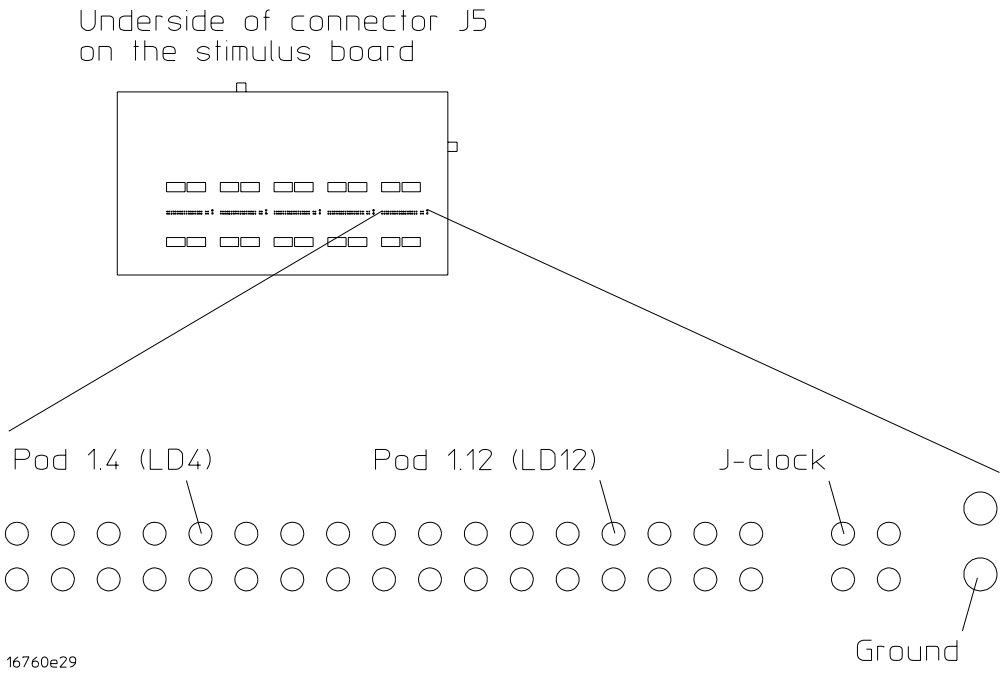
c Connect one end of an SMA cable to the channel 2 input of the oscilloscope. Connect the free end of the SMA cable to one 54006A probe.



2 Determine the output threshold levels.

a Enable the pulse generator Channel 1 OUTPUT, channel 2 OUTPUT, and trigger OUTPUT (LED off).

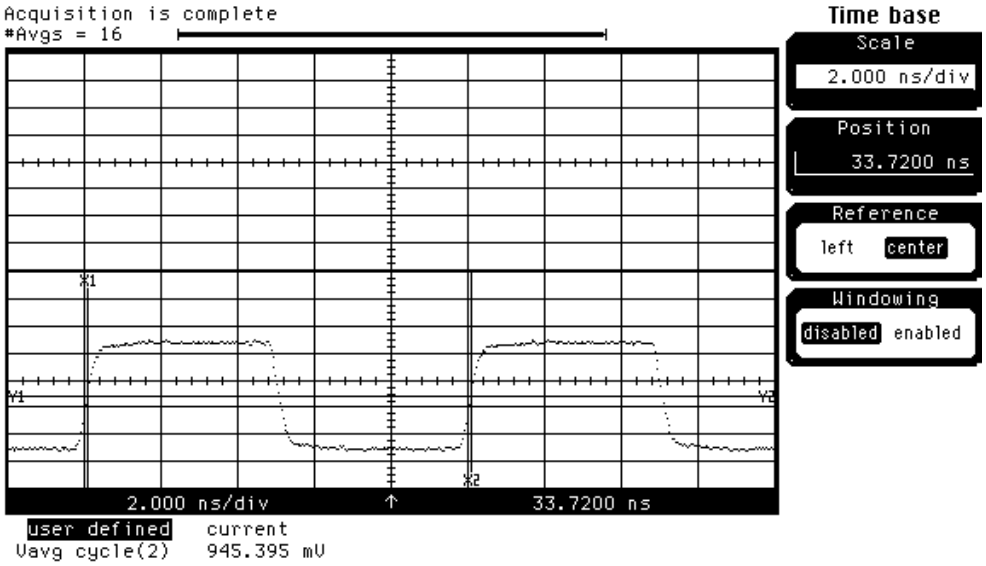
Use the following diagram for the next steps.



b Using oscilloscope channel 2, probe the J-clock signal on the underside of the stimulus board.

c Adjust the oscilloscope Timebase: Position until a rising edge appears on the left of the display.

d On the oscilloscope, select [Shift] More meas, then select V avg. then select [Enter]. Select Source, then select Channel 2. Read the Vavg cycle(2) value on the oscilloscope display.



e Round the Vavg cycle(2) value to the nearest 10 mV and write it here: Vavg cycle(2) = _____ mV = V_{thresh}

In the above figure, Vavg cycle(2) = 950mV = V_{thresh}

3 Reconfigure the oscilloscope channel and marker thresholds.

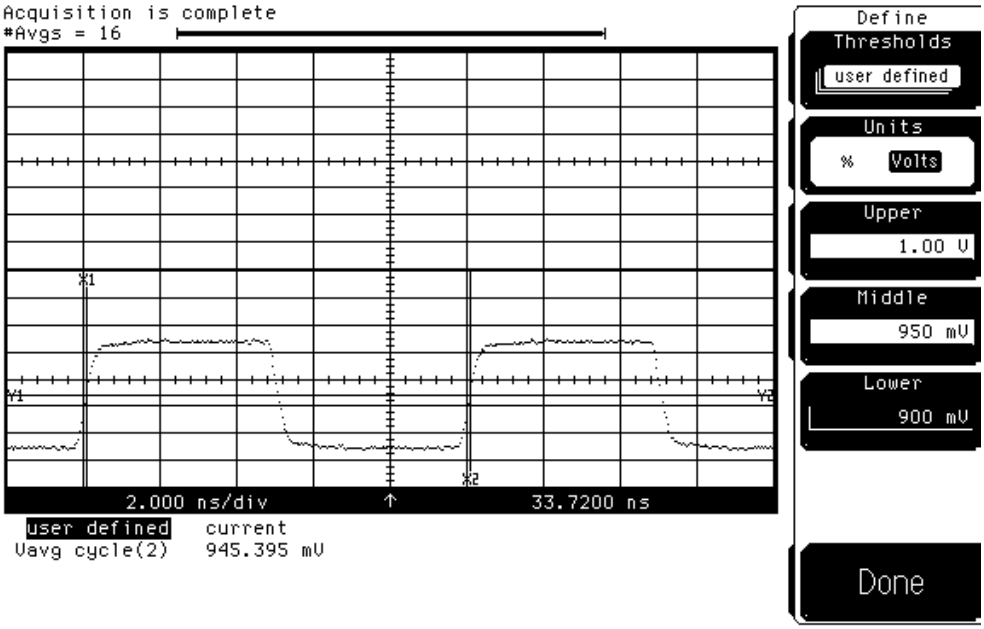
a In the oscilloscope channel 1 menu, select the Offset field. Enter the V_{thresh} value you wrote in step 2e above.

b Repeat the above step for oscilloscope channel 2.

c On the oscilloscope, select [Define meas], then select Thresholds user defined... Set the Upper, Middle, and Lower marker thresholds according to the following table:

Middle	Same Voltage as the V_{thresh} measured above
Upper	V_{thresh} + 50mV
Lower	V_{thresh} - 50mV

If V_{thresh} was measured at 950mV above, then Middle is set to 950mV, Upper is set to 1.000V, and Lower is set to 900mV.



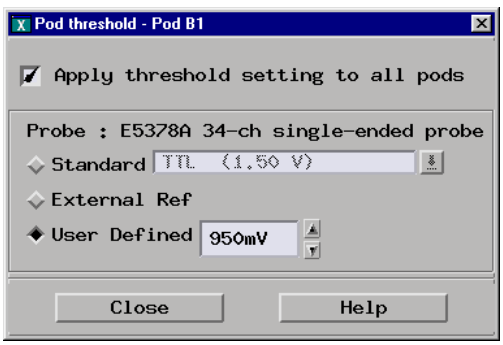
4 Reconfigure the logic analyzer thresholds to the output threshold levels.

a In the logic analyzer Setup and Trigger window, select the Format tab.

b Under the Format tab, select the threshold field under either pod. The Pod threshold window will appear.

c In the Pod threshold window, ensure Apply threshold setting to all pods is checked.

d In the Pod threshold window, select User Defined, then select the threshold voltage field. Enter the V_{thresh} value you wrote in step 2e above.

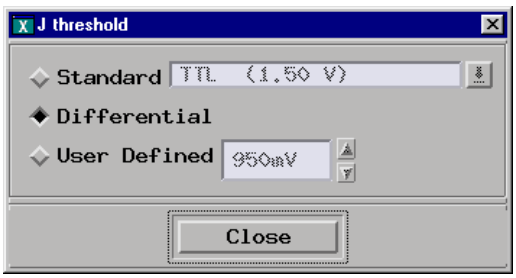


e Select Close to close the Pod threshold window.

f Under the Format tab, select Clk Thresh... field. the Clock threshold window will appear.

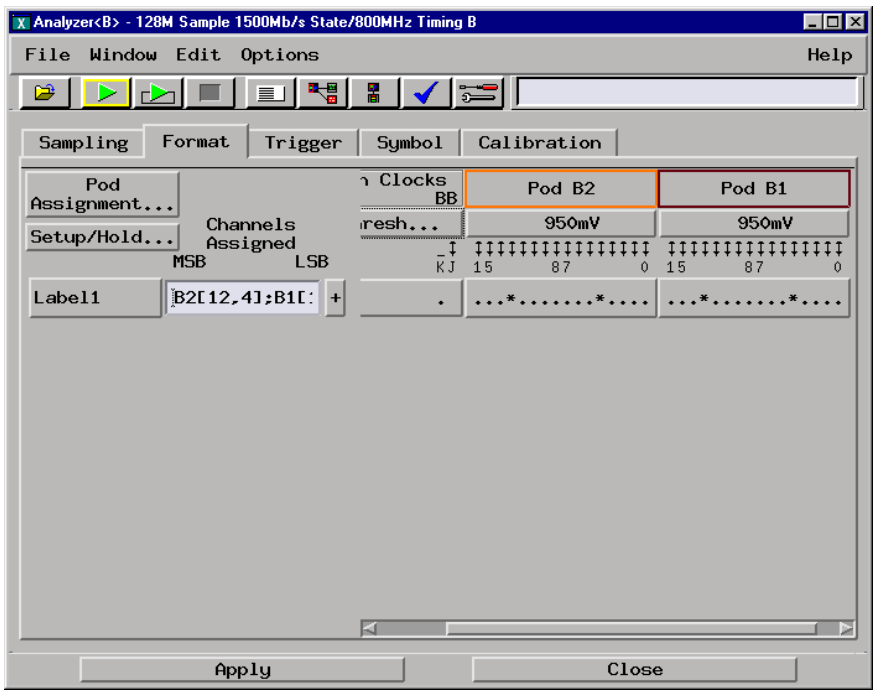
g Select the threshold field associated with J clock. The J threshold window will appear.

h In the J threshold window, select Differential.



i Select Close to close the J threshold window, then select Close to close the Clock threshold window.

Both pods and the J clock should now show activity.



Validating state mode test failures

Do the following procedure only if one of the state mode tests results in unexpected test data. The procedure provides hints on how to verify if the unexpected test data is the result of a hardware failure of the module.

Do the following steps in this order:

- Verify ETE settings and configuration
- Verify pulse timing parameters on the stimulus board
- Verify the stimulus board operating threshold voltages

Verify ETE settings and configuration

1 Check the pulse generator settings.

Begin with “To Set up the Test Equipment and the Analyzer” on page 35 to ensure the pulse parameter settings on the pulse generator are configured correctly. Then modify the pulse parameters if so indicated at the beginning of the test. The only pulse generator settings changed are Period and Delay.

2 Check the cabling.

Again, verify the stimulus board and the logic analyzer are cabled correctly according to “To Set up the Test Equipment and the Analyzer” on page 35. Also, make sure the stimulus board power is on.

For the multicard test, verify that the logic analyzer cables are connected properly to the Agilent E5378A. If the test data is correct but out of sequence (for example, "1A" and "25"), this indicates the cables of one of the modules is connected backwards. Reconnect the cables to the E5378A probe adapter so logic analyzer Pod 1 is connected to the probe adapter "Odd" connector and Pod 2 is connected to "Even". Note that in the Setup and Trigger window under the Format tab, you must reconfigure the Clock Thresh... to Differential.

3 Check the module settings.

Review the procedure to verify the module Setup and Trigger window is configured correctly to acquire the data.

Verify pulse timing parameters on the stimulus board

If the error message "Pattern NOT found for marker <Gn> - last occurrence at nnnn" appears, then the most likely cause is the pulse generator channel Delay is incorrectly set. The magnitude of the error in the pulse generator Delay is shown by the "last occurrence at nnnn" number. If the number is close to the 4095 count of expected occurrences, then the error in the pulse generator Delay is small.

The stimulus board is designed for optimum signal fidelity and stability. Also, The 8133A #003 tends to be both precise and accurate, therefore routine monitoring with an oscilloscope is not necessary. Although the Agilent 16760A module is designed with sufficient guardband in the specifications, verifying the stimulus board signals with an oscilloscope will ensure the expected pulse parameters are correct as the signals are being fed to the logic analyzer module.

Do the procedure “Characterize the stimulus board output threshold” on page 52 to measure the time delay between the data pulse and the clock pulse (ΔTime(1)-(2)). Ensure the ΔTime(1)-(2) value as the same as the value entered into the Setup: field of the Sampling Positions window. Make appropriate adjustments to the pulse generator Channel 2 Delay.

Verify the stimulus board operating threshold voltages

If the Setup and Trigger window Format tab displays no activity on the pod activity indicators, the most likely cause is the logic analyzer threshold voltage is not properly configured.

Do the procedure “Characterize the stimulus board output threshold” on page 52 to measure the stimulus board operating threshold voltages.

To test double-edge clocking modes

Testing double-edge clocking modes verifies both maximum state acquisition speed and the double-edge clocking mode setup/hold times.

Set up the equipment

If you have not already done so, do the following procedures:

- "To Set up the Test Equipment and the Analyzer" on page 35
- "To configure the analyzer for the state mode tests" on page 46
- "Characterize the stimulus board output threshold" on page 52

Check 200 Mb/s state acquisition speed

This test verifies both the maximum state speed and hold time.

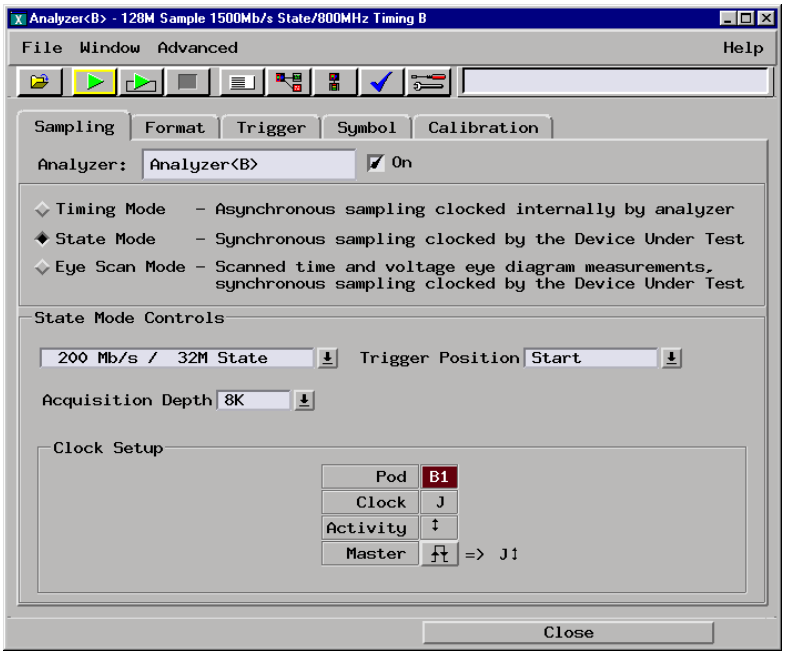
1 Configure the pulse generator.

- 0 ps delay on Channel 2
- 5.000 ns period

2 Configure the logic analyzer.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

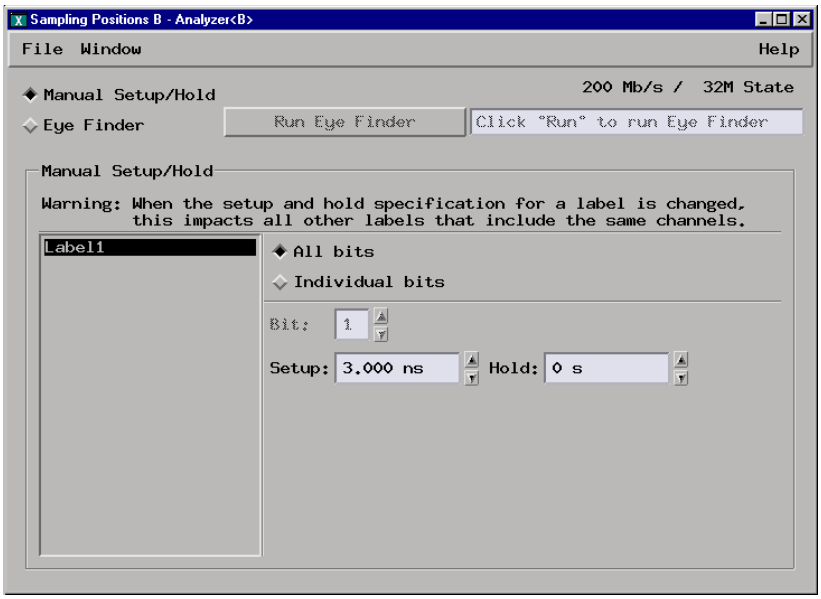
b Under the Sampling tab, select the State Mode selection field, then select 200 Mb/s / 32M State.



c In the logic analyzer Setup and Trigger window, select the Format tab. Under the Format tab, select Setup/Hold... The Sampling Positions window will appear.

d In the Sampling Positions window, ensure All bits is selected.

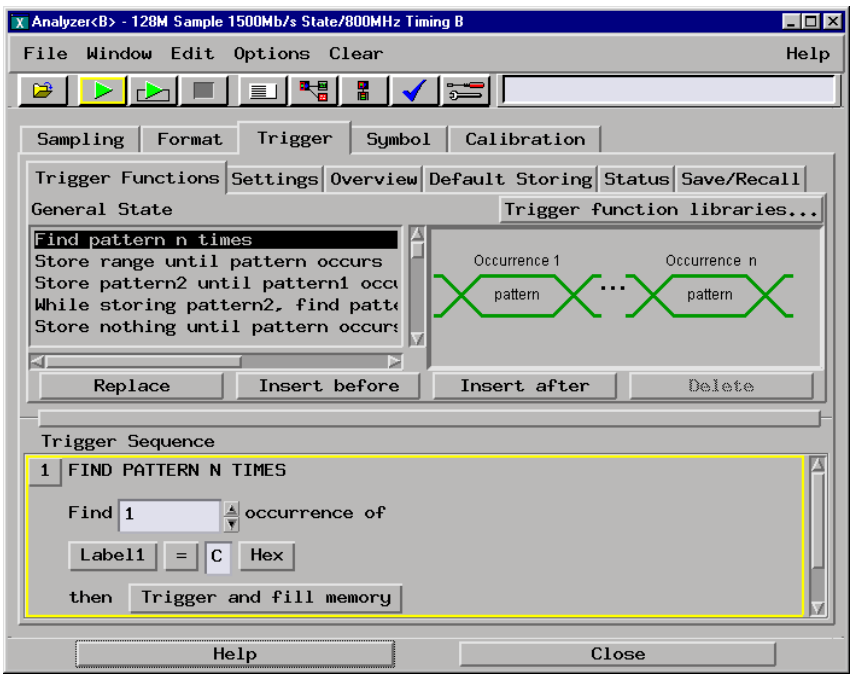
e Enter a setup time 3.000ns then press the [Enter] key. The Hold: field should display “0 s”.



3 Configure the Trigger pattern.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger Sequence, locate the Label1 = trigger pattern field. Enter "C" in the trigger pattern field. The trigger function should now read Find 1 occurrence of Label1 = C Hex then Trigger and fill memory.



4 Verify the test data.

a In the Listing window, select the Run icon.

b If you have not already done so, do step 6 of "To configure the analyzer for the state mode tests" on page 50 (this will clear the Pattern not found error message).

c The test passes if no error messages appear and the test data appears as explained in step 6 of "To configure the analyzer for the state mode tests" on page 50. If an error message appears, refer to Validating state mode test failures.

Check 200 Mb/s double-edge clock setup time

1 Adjust the pulse generator channel 2 delay to 2.000 ns.

2 Verify the test data.

a In the Listing window, select the Run icon.

b The test passes if no error messages appear and the test data appears as explained in step 6 of "To configure the analyzer for the state mode tests" on page 46. Record a Pass in the Performance Test Record.

c If an error message appears, refer to Validating state mode test failures.

3 Return the pulse generator channel 2 delay setting to 0 ps.

Check 400 Mb/s state acquisition

1 Configure the pulse generator.

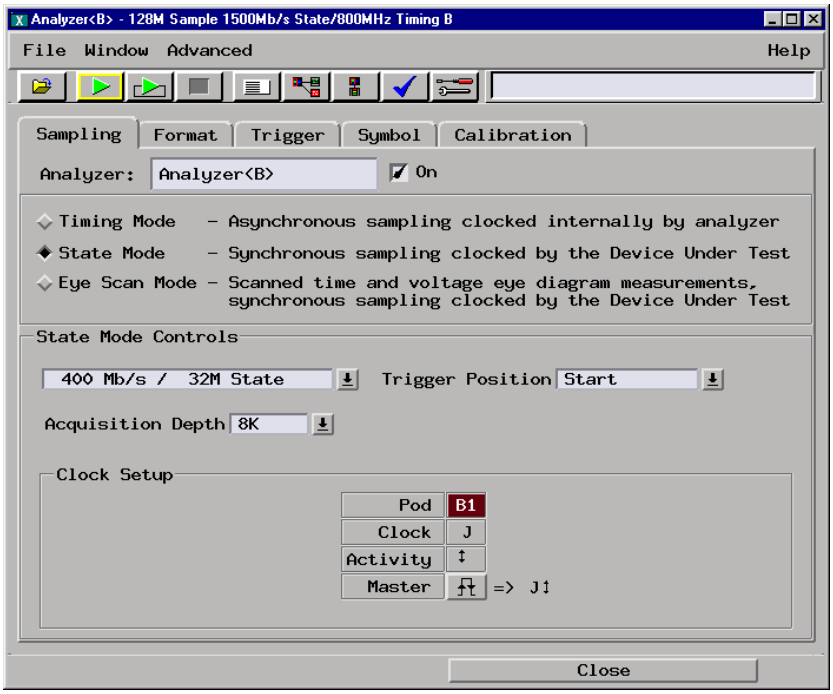
- 0 ps delay on Channel 2
- 2.500 ns period

2 Configure the logic analyzer.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select the State Mode selection field, then select 400 Mb/s / 32M State.

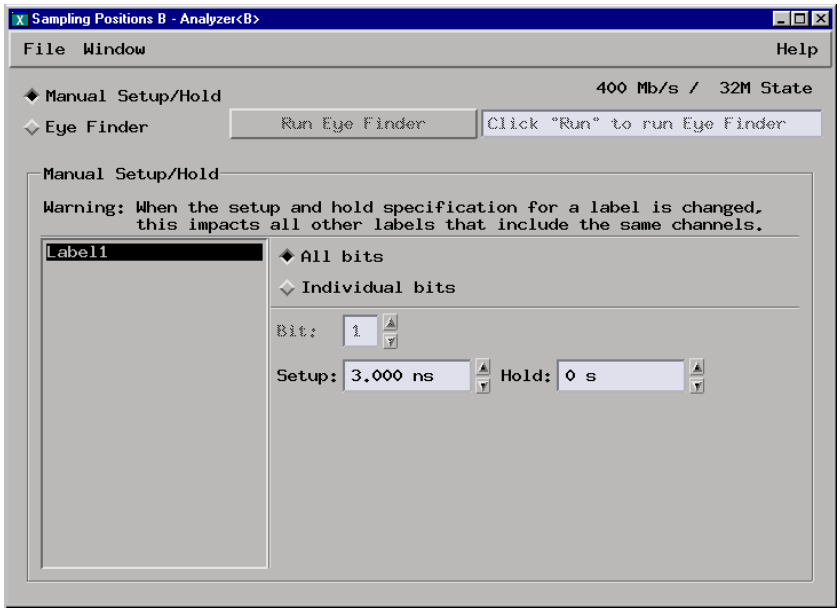
c Select the clock edge field for J-clock, then select Both Edges.



d In the logic analyzer Setup and Trigger window, select the Format tab. Under the Format tab, select Setup/Hold... The Sampling Positions window will appear.

e In the Sampling Positions window, ensure All bits is selected.

f Enter a setup time of 3.000 ns then press the Enter key. The Hold: field should display “0 s”.

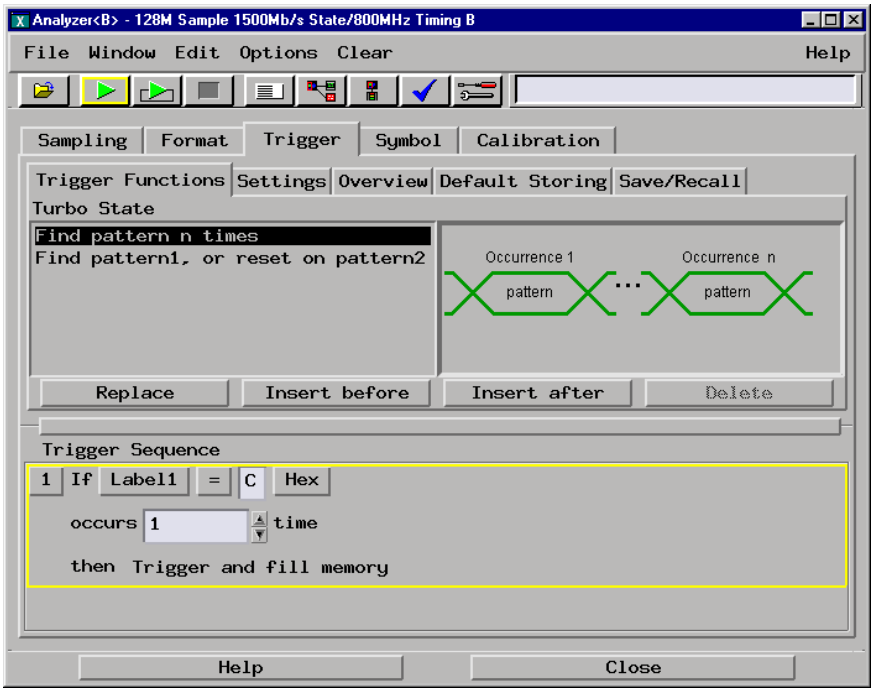


3 Configure the Trigger pattern.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Ensure the Find pattern n times trigger function is selected. If not, click Find pattern n times to select, then select Replace.

c Under Trigger Sequence, locate the Label1 = trigger pattern field. Enter "C" in the trigger pattern field. The trigger function should now read If Label1 = C Hex occurs 1 time then Trigger and fill memory.



4 Verify the test data.

a In the Listing window, select the Run icon.

b If you have not already done so, do step 6 of "To configure the analyzer for the state mode tests" on page 50.

c The test passes if no error messages appear and the test data appears as explained in step 6 of "To configure the analyzer for the state mode tests" on page 50. If an error message appears, refer to Validating state mode test failures.

Check 400 Mb/s double-edge setup time

1 Adjust the pulse generator channel 2 delay to 2.000 ns.

2 Verify the test data.

a In the Listing window, select the Run icon.

b The test passes if no error message appears and the test data appears as explained in step 6 of "To configure the analyzer for the state mode tests" on page 46. Record a Pass in the Performance Test Record.

c If an error message appears, refer to Validating state mode test failures.

3 Return the pulse generator channel 2 delay setting to 0 ps.

Check 800 Mb/s state acquisition speed and setup time

The design of the stimulus board and a 0 ps delay in the pulse generator configuration cause the signal to be properly configured for verifying both setup time and hold time in addition to maximum state acquisition speed without increasing the channel 2 (data) delay value.

1 Configure the pulse generator.

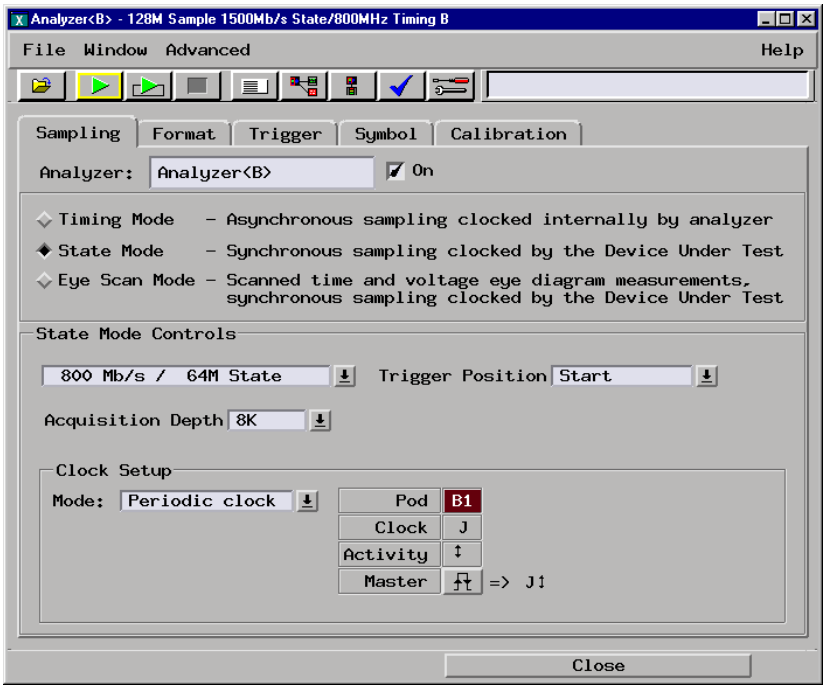
- 0 ps delay on Channel 2
- 1.250 ns period

2 Configure the logic analyzer.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select the State Mode selection field, then select 800 Mb/s / 64M State.

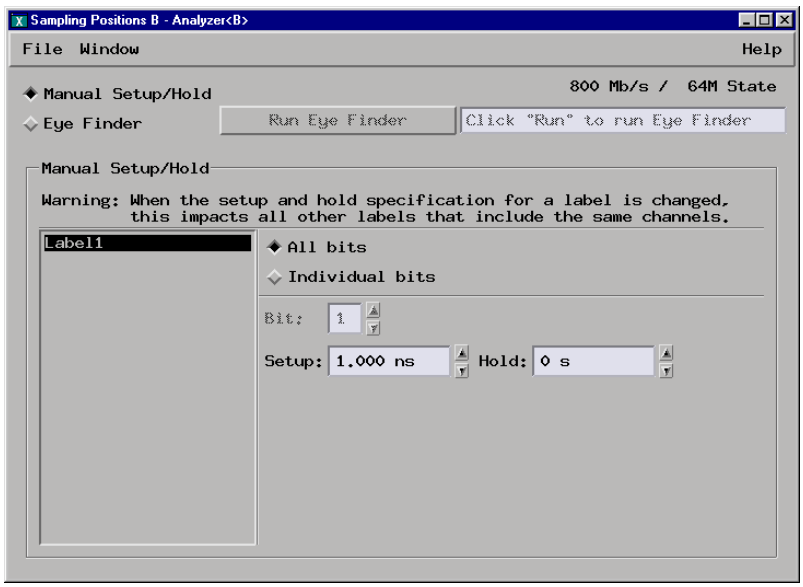
c Select the clock edge field for J-clock, then select Both Edges.



d In the logic analyzer Setup and Trigger window, select the Format tab, then select Setup/Hold... The Sampling Positions window will appear.

e In the Sampling Positions window, ensure All bits is selected.

f Enter a setup time of 1.000 ns then press the [Enter] key. The Hold: field should display “0 s”.



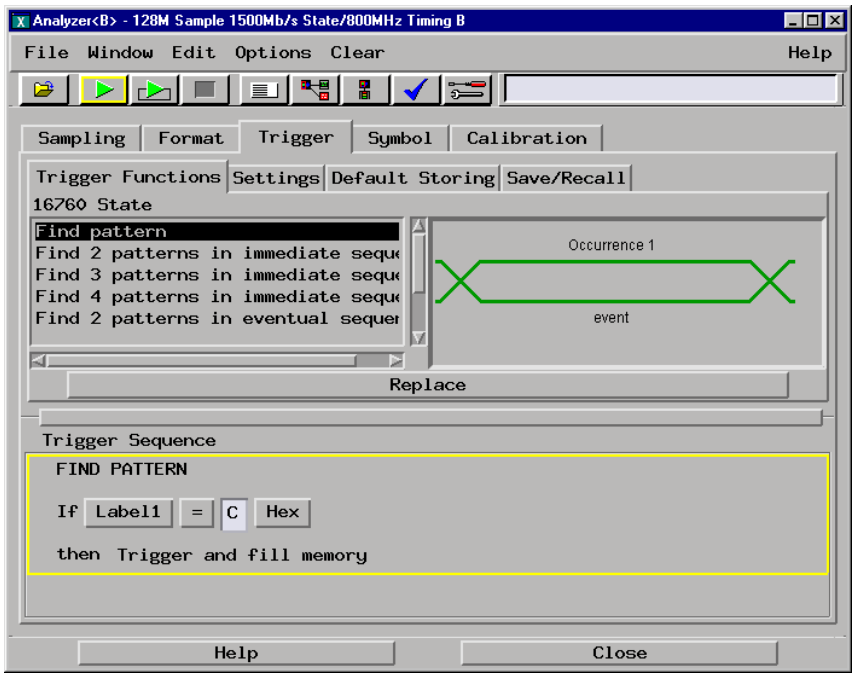
3 Configure the Trigger pattern.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger Functions tab, ensure the Find Pattern trigger function is selected. If not, click Find pattern to select, then select Replace.

c If the trigger function reads If Anything, do the following steps: Select Anything, then select Replace Event. At the pop-up, select Label. At the Label pop-up window, select Label1, then select OK.

d Under Trigger Sequence, locate the Label1 = trigger pattern field. Enter "C" in the trigger pattern field. The trigger function should now read If Label1 = C Hex then Trigger and fill memory.



4 Verify the test data.

a In the Listing window, select the Run icon.

b If you have not already done so, do step 6 "To configure the analyzer for the state mode tests" on page 50.

c The test passes if no error messages appear and the test data appears as explained in step 6 of "To configure the analyzer for the state mode tests" on page 50. If an error messages appears, refer to Validating state mode test failures.

To test single-edge setup/hold window

Set up the equipment

1 If you have not already done so, do the following procedures:

- "To Set up the Test Equipment and the Analyzer" on page 35
- "To configure the analyzer for the state mode tests" on page 46
- "Characterize the stimulus board output threshold" on page 52

2 Configure the pulse generator for single-edge tests.

Timebase	Channel 2	Trigger	Channel 1
Mode: Int Period: 5.000 ns	Mode: Pulse Divide: Pulse ÷ 2 Width: 2.500 ns Ampl: 0.80 V Offs: 2.00 V COMP: Disabled (LED Off)	Divide: Divide ÷ 2 Ampl: 0.50 V Offs: 0.00 V	Mode: Square Delay: 0.000 ns Ampl: 0.80 V Offs: 2.00 V COMP: Disabled (LED Off)

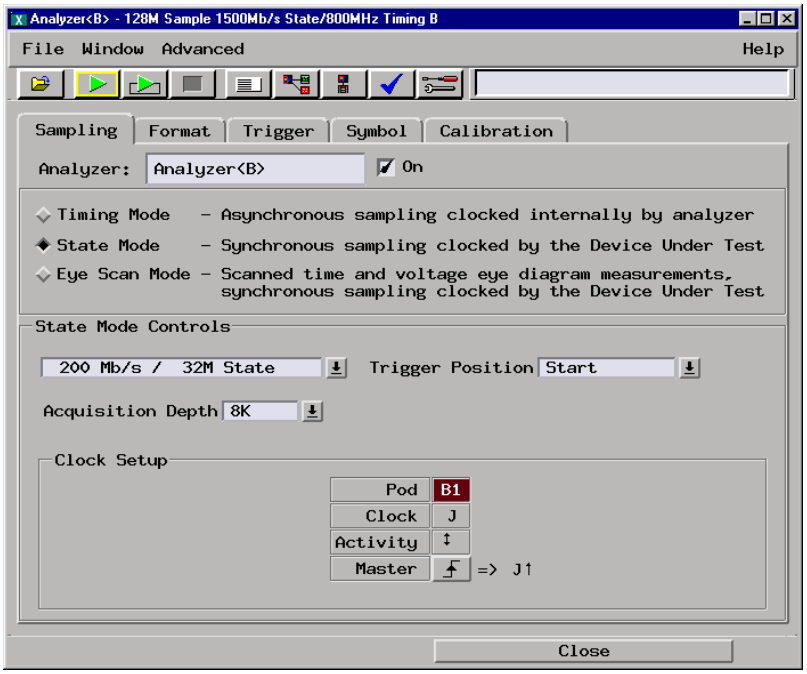
Check 200 Mb/s single-edge hold time

1 Configure the logic analyzer.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select the State Mode selection field, then select 200 Mb/s / 32M State.

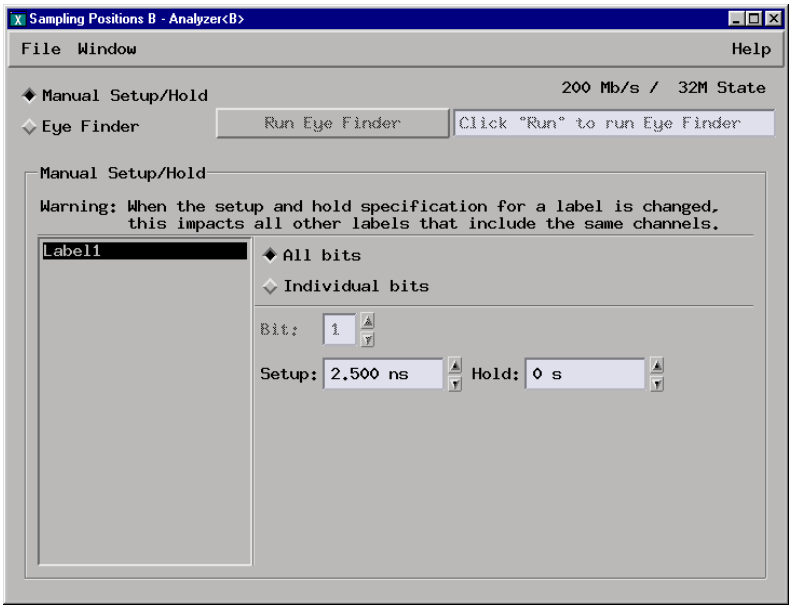
c Select the clock edge field for J-clock, then select Rising Edge.



d In the logic analyzer Setup and Trigger window, select the Format tab. Under the Format tab, select Setup/Hold... The Sampling Positions window will appear.

e In the Sampling Positions window, ensure All bits is selected.

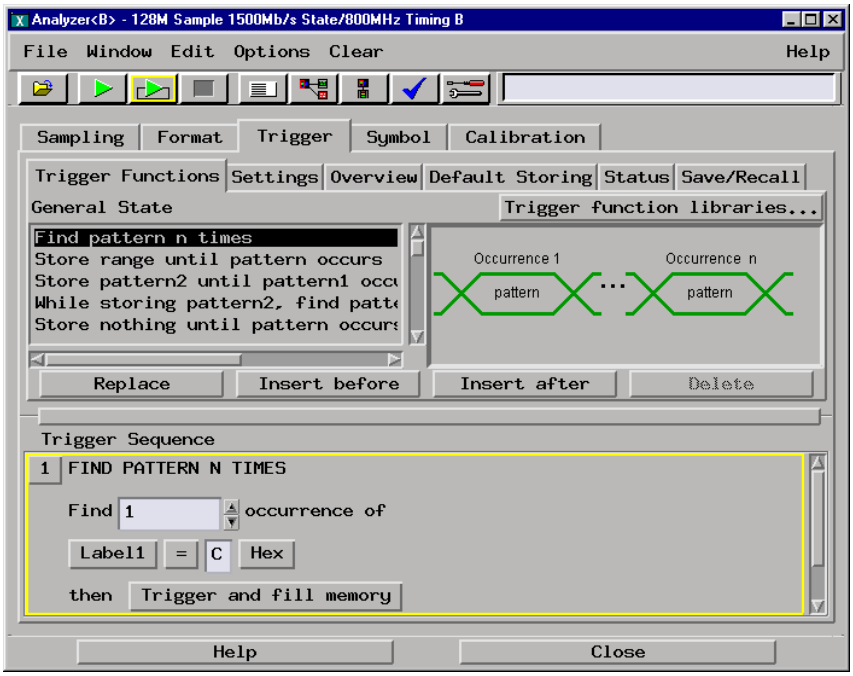
f Enter a setup time of 2.500 ns then press the Enter key. The Hold: field should display “0 s”.



2 Configure the Trigger pattern.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger Sequence, locate the Label1 = trigger pattern field. Enter “C” in the trigger pattern field. The trigger function should now read Find 1 occurrence of Label1 = C Hex then Trigger and fill memory.



3 Verify the data.

a In the Listing window, select the Run icon.

b If you have not already done so, do step 6 of “To configure the analyzer for the state mode tests” on page 46.

c The test passes if no error messages appear and the test data appears as explained in step 6 of “To configure the analyzer for the state mode tests” on page 46. If an error message appears, refer to Validating state mode test failures.

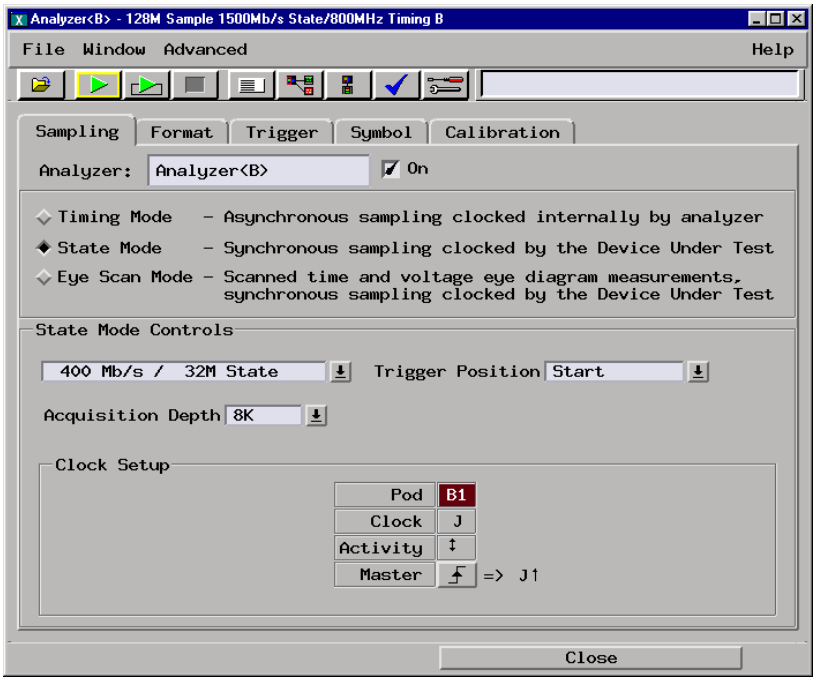
Check 400 Mb/s single-edge hold time

1 Configure the logic analyzer.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select the State Mode selection field, then select 400 Mb/s / 32M State.

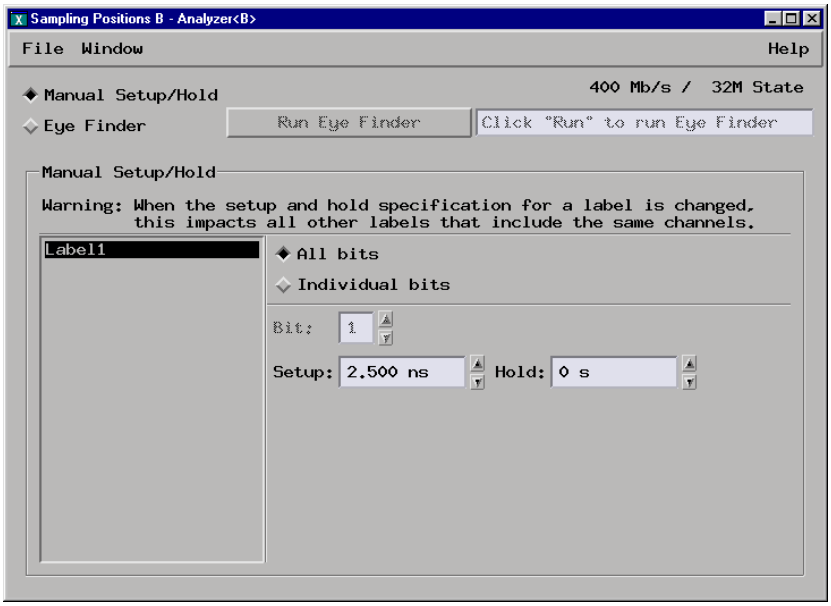
c Select the clock edge field for J-clock, then Rising Edge.



d In the logic analyzer Setup and Trigger window, select the Format tab. Under the Format tab, select Setup/Hold... The Sampling Positions window will appear.

e In the Sampling Positions window, ensure All bits is selected.

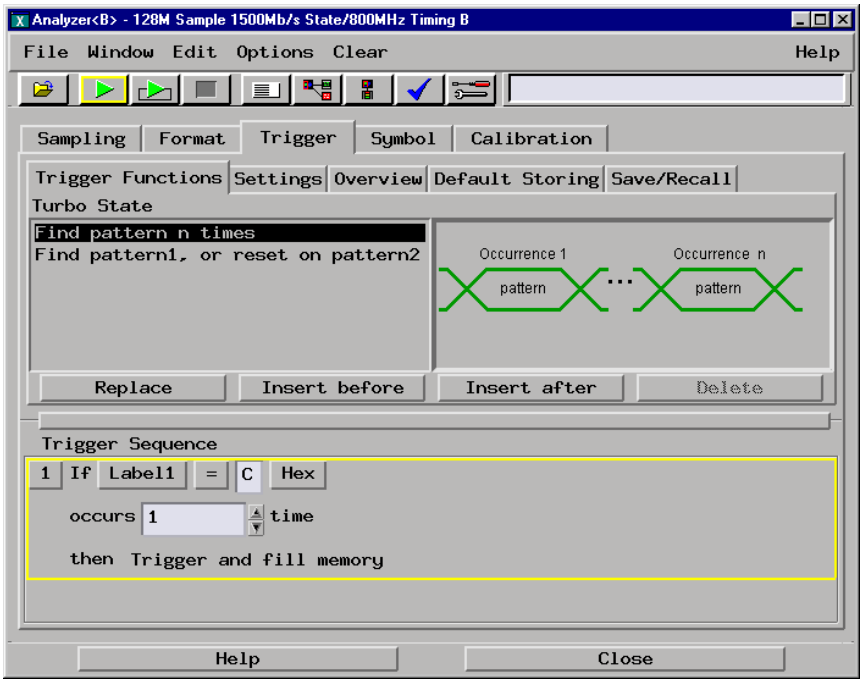
f Enter a setup time of 2.500 ns then press the Enter key. The Hold: field should display “0 s”.



2 Configure the Trigger pattern.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger Sequence, locate the Label1 = trigger pattern field. Enter “C” in the trigger pattern field. The trigger function should now read If Label1 = C Hex occurs 1 time then Trigger and fill memory.



3 Verify the data.

a In the Listing window, select the Run icon.

b If you have not already done so, do step 6 of "To configure the analyzer for the state mode tests" on page 46.

c The test passes if no error messages appear and the test data appears as explain in step 6 of "To configure the analyzer for the state mode tests" on page 46. If an error message appears, refer to Validating state mode test failures.

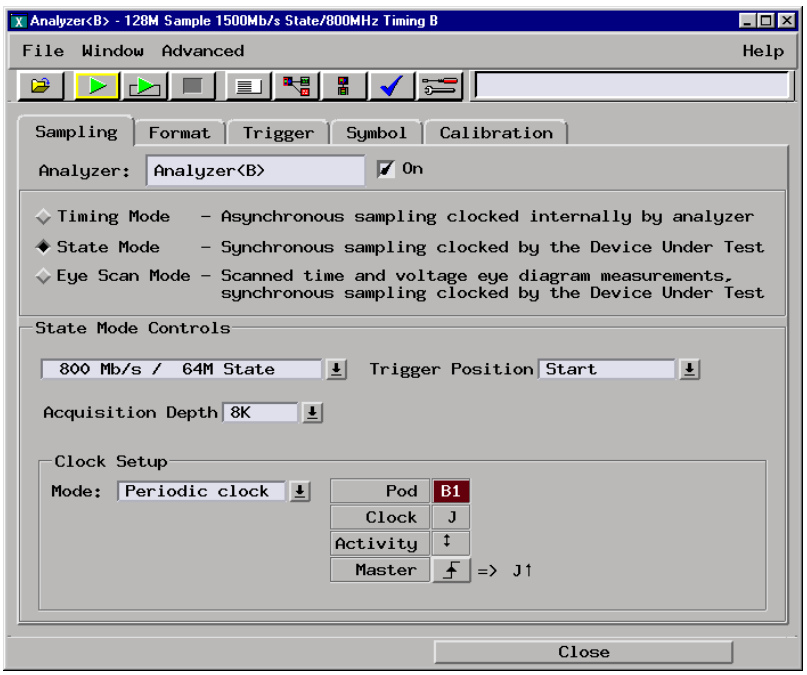
Check 800 Mb/s single-edge hold time

1 Configure the logic analyzer.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select the State Mode selection field, then select 800 Mb/s /32M State.

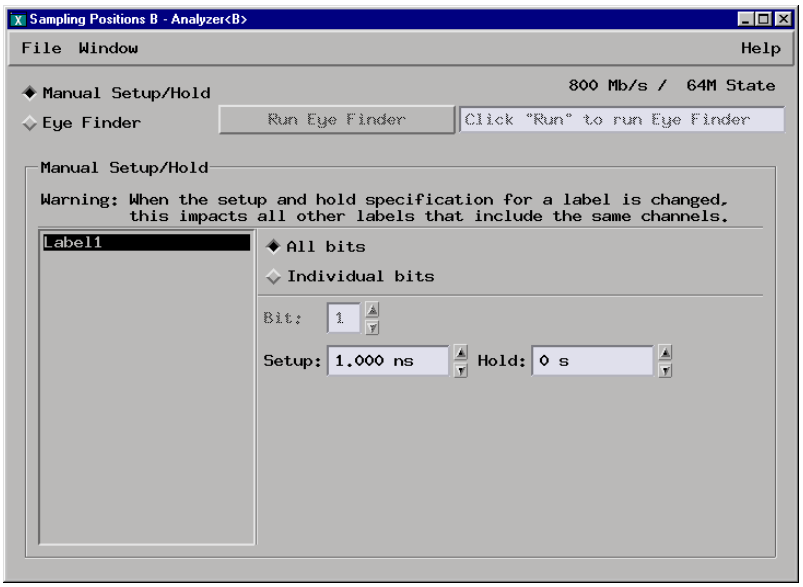
c Select the clock edge field for J-clock, then Rising Edge.



d In the logic analyzer Setup and Trigger window, select the Format tab. Under the Format tab, select Setup/Hold... The Sampling Positions window will appear.

e In the Sampling Positions window, ensure All bits is selected.

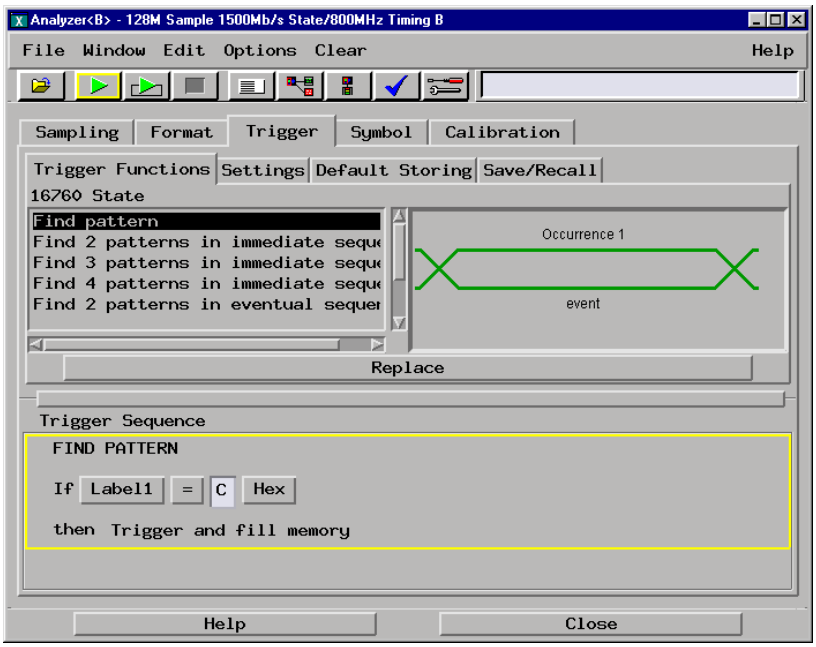
f Enter a setup time of 1.000 ns then press the Enter key. The Hold: field should display “0 s”.



2 Configure the Trigger pattern.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger Sequence, locate the Label1 = trigger pattern field. Enter “C” in the trigger pattern field. The trigger functions should now read If Label1 = C Hex then Trigger and fill memory.



3 Verify the test data.

a In the Listing window, select the Run icon.

b If you have not already done so, do step 6 of "To configure the analyzer for the state mode tests" on page 46.

c The test passes if no error messages appear and the test data appears as explained in step 6 of "To configure the analyzer for the state mode tests" on page 46.

Check 200 Mb/s single-edge setup time

1 Configure the pulse generator.

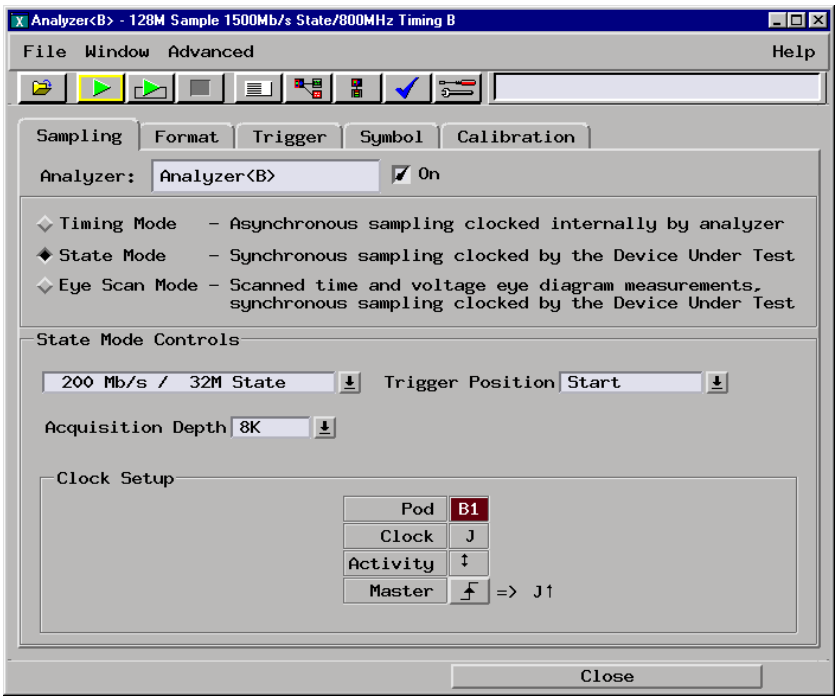
- 2.500 ns delay on Channel 2

2 Configure the logic analyzer.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select the State Mode selection field, then select 200 Mb/s /32M State.

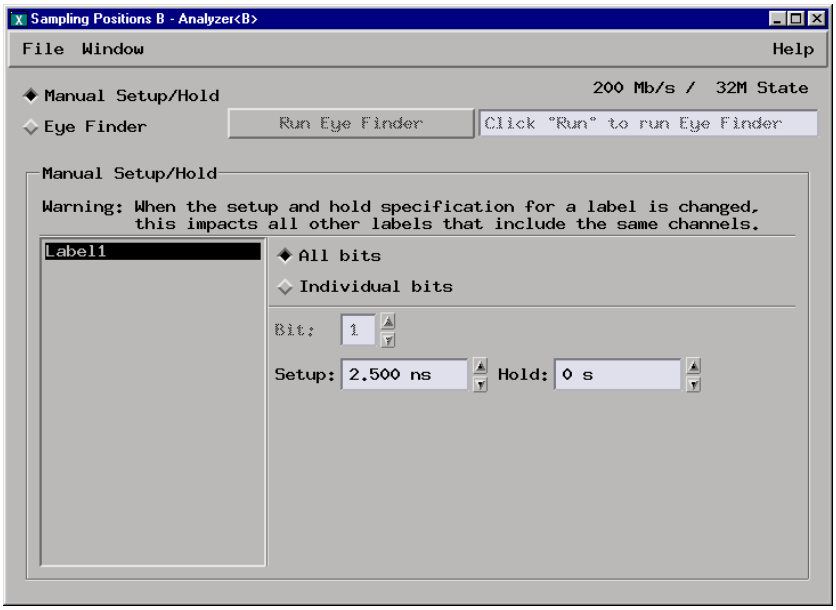
c Select the clock edge field for J-clock, then select Rising Edge.



d In the logic analyzer Setup and Trigger window, select the Format tab. Under the Format tab, select Setup/Hold... The Sampling Positions window will appear.

e In the Sampling Positions window, ensure All bits is selected.

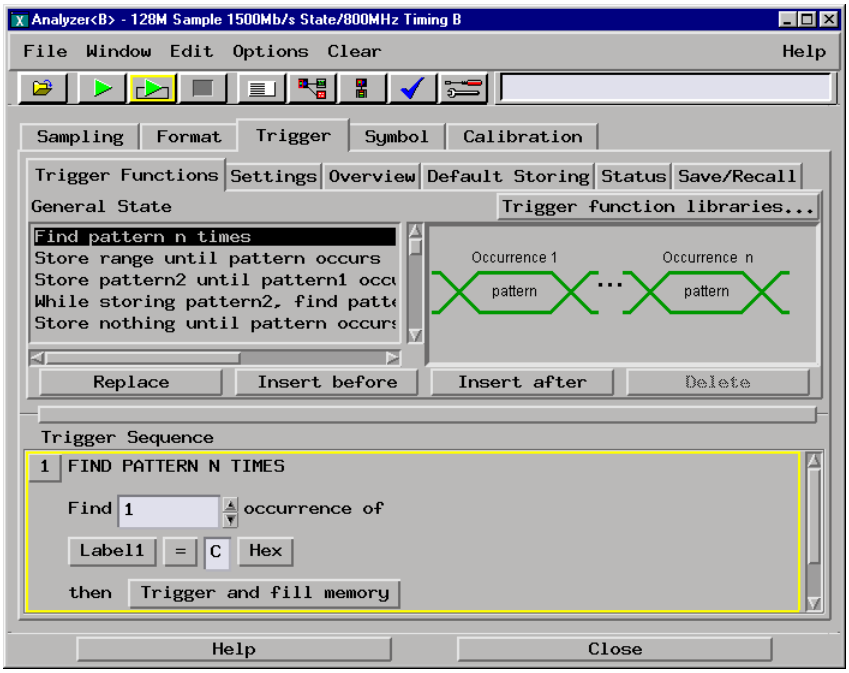
f Enter a setup time of 2.500 ns then press the Enter key. The Hold: field should display “0 s”.



3 Configure the Trigger pattern.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger Sequence, locate the Label1 = trigger pattern field. Enter "C" in the trigger pattern field. The trigger function should now read Find 1 occurrence of Label1 = C Hex then Trigger and fill memory.



4 Verify the test data.

a In the Listing window, select the Run icon.

b If you have not already done so, do step 6 of "To configure the analyzer for the state mode tests" on page 46.

c The test passes if no error messages appear and the test data appears as explained in step 6 of "To configure the analyzer for the state mode tests" on page 46. If an error message appears, refer to Validating state mode test failures.

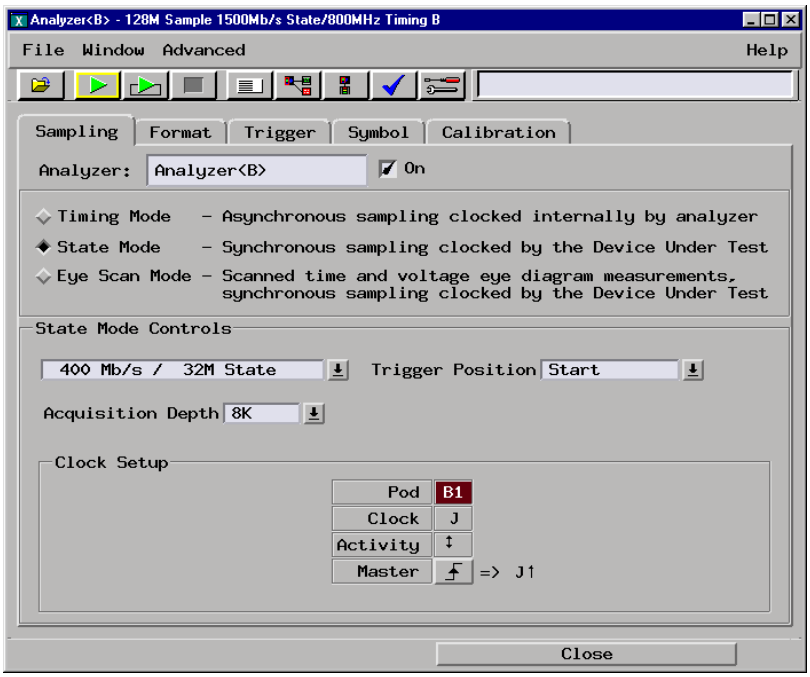
Check 400 Mb/s single-edge setup time

1 Configure the logic analyzer.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select the State Mode selection field, then select 400 Mb/s / 32M State.

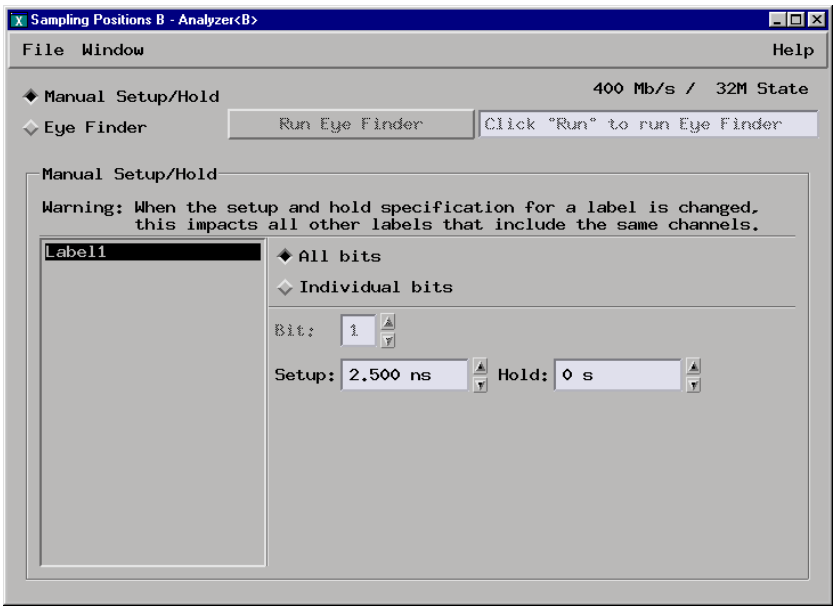
c Select the clock edge field for J-clock, then select Rising Edge.



d In the logic analyzer Setup and Trigger window, select the Format tab. Under the Format tab, select Setup/Hold... The Sampling Positions window will appear.

e In the Sampling Positions window ensure All bits is selected.

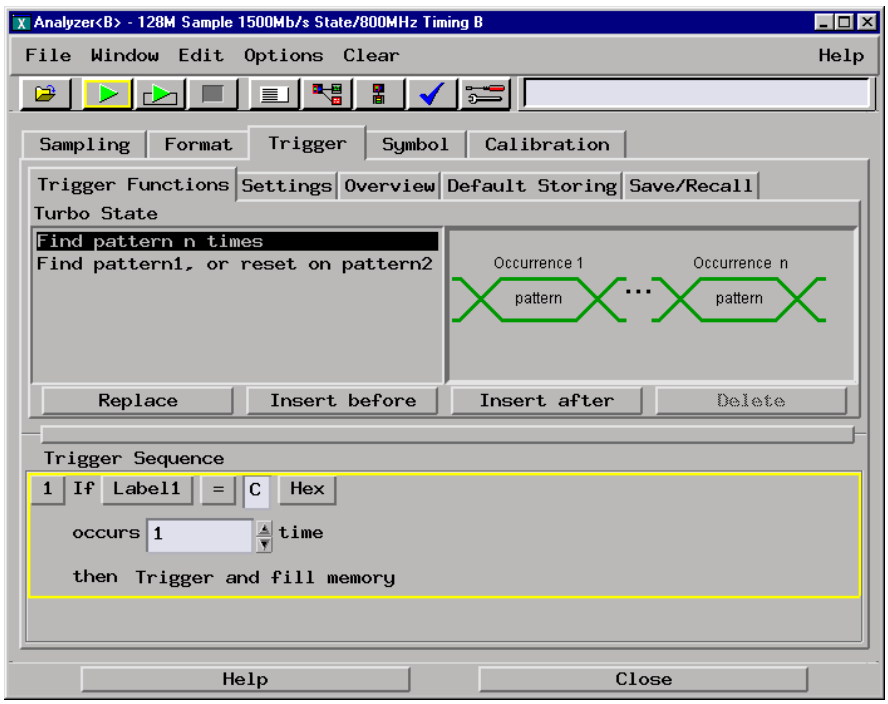
f Enter a setup time of 2.500 ns then press the Enter key. The Hold: field should display “0 s”.



2 Configure the Trigger pattern.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under Trigger Sequence, locate the Label1 = trigger pattern field. Enter "C" in the trigger pattern field. The trigger function should now read If Label1 = C Hex occurs 1 time then Trigger and fill memory.



3 Verify the test data.

a In the Listing window, select the Run icon.

b If you have not already done so, do step 6 "To configure the analyzer for the state mode tests" on page 46".

c The test passes if no error messages appear and the test data appear as explained in step 6 of "To configure the analyzer for the state mode tests" on page 46. If an error messages appears, refer to Validating state mode test failures.

Check 800 Mb/s single-edge setup time

1 Configure the pulse generator.

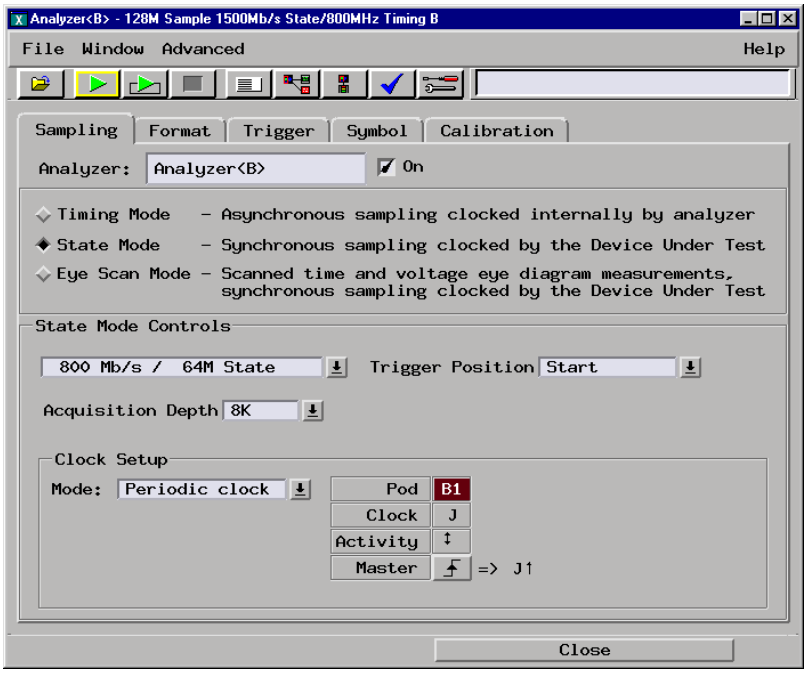
- 4.000 ns delay on Channel 2

2 Configure the logic analyzer.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select the State Mode selection field, then select 800 Mb/s /32M State.

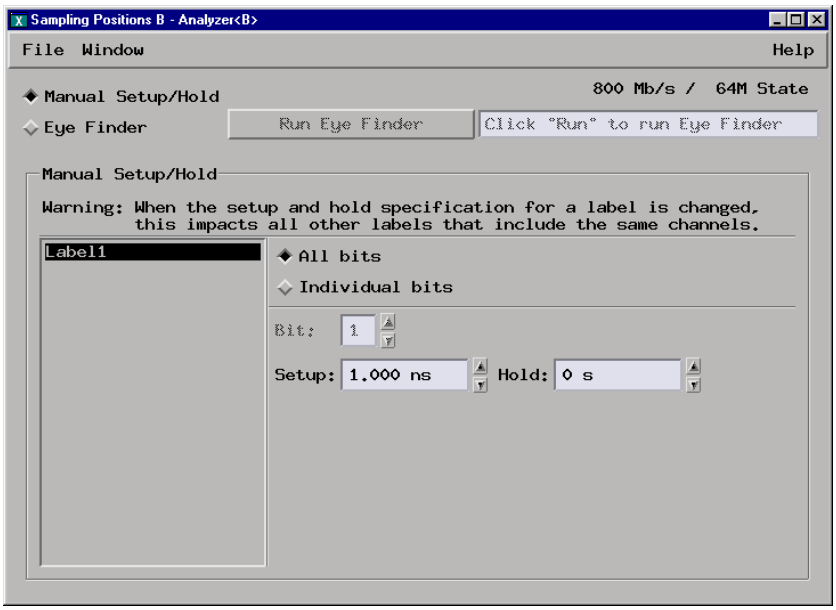
c Select the clock edge field for J-clock, then select Rising Edge.



d In the logic analyzer Setup and Trigger window, select the Format tab, then select Setup/Hold... The Sampling Positions window will appear.

e In the Sampling Positions window, ensure All bits is selected.

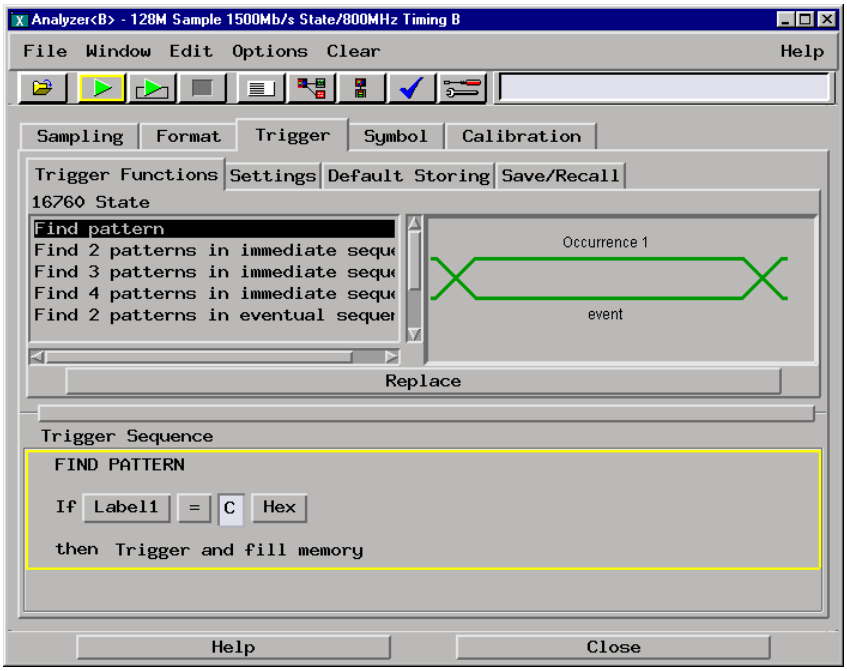
f Enter a setup time of 1.000 ns then press the Enter key. The Hold: field should display “0 s”.



3 Configure the Trigger pattern.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger Sequence, locate the Label1 = trigger pattern field. Enter “C” in the trigger pattern field. The trigger function should now read If Label1 = C Hex then Trigger and fill memory.



4 Verify the test data.

a In the Listing window, select the Run icon.

b If you have not already done so, do step 6 of "To configure the analyzer for the state mode tests" on page 46.

c The test passes if no error messages appear as explained in step 6 of "To configure the analyzer for the state mode tests" on page 46. If an error message appears, refer to Validating state mode test failures.

5 End the state mode tests.

a In the Listing window, select the [x] field in the upper right hand corner of the window to close the window.

b In the Setup and Trigger window, select the [x] field in the upper right hand corner of the window to the close the window.

c In the Logic Analysis System window, select the [x] field in the upper right hand corner of the window to close the window.

Ending and restarting the logic analysis session will reinitialize the system for the time interval accuracy test.

To Test the 1500 Mb/s state acquisition mode

Because of the speeds involved, this test verifies the low byte then the high byte of each pod. Do this procedure for the low byte by checking channel 4 of each pod, then repeat the procedure for channel 12 of each pod.

Set up the equipment

If you have not already done so, do the following procedures:

- "To Set up the Test Equipment and the Analyzer" on page 35
- "To configure the analyzer for the state mode tests" on page 46
- "Characterize the stimulus board output threshold" on page 52

Characterize the stimulus board delay

1 Configure the pulse generator.

- 0 ps delay on channel 2 and channel 1
- 666 ps period

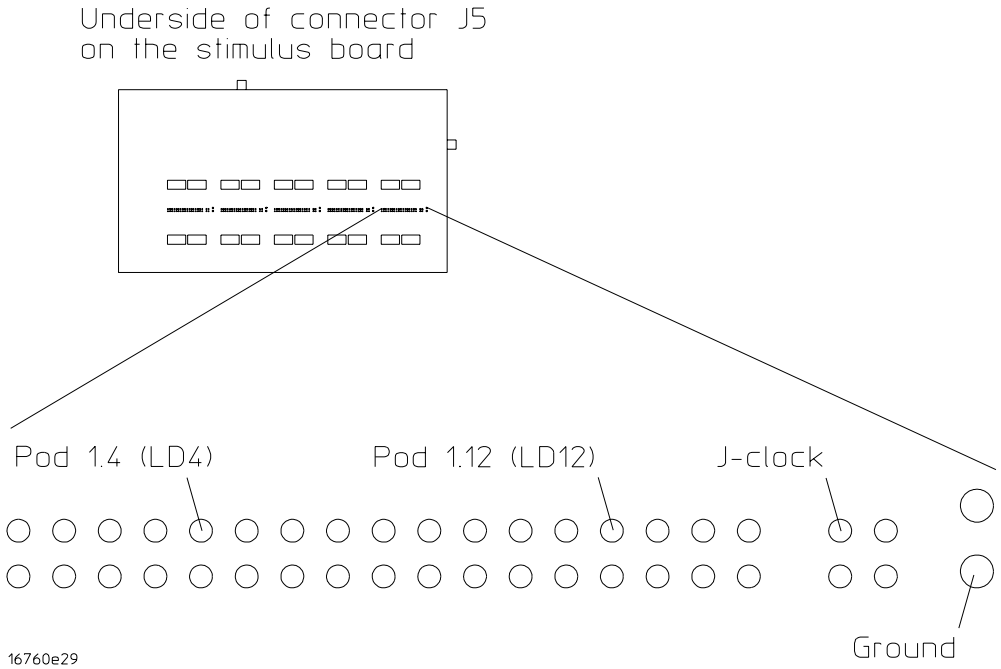
2 Measure the data signal delay of the stimulus board.

Because of the speeds involved, you must ensure the data and clock test signals are closely aligned according to the setup time configured under the Format tab in the Setup and Trigger window. Once you have measured the delay value, it can be used for all future calibrations. After measuring the delay in the next step, write the value here:

Channel 1 delay: _____ ps for LD4

Channel 1 delay: _____ ps for LD12

Use the following diagram for the next steps:



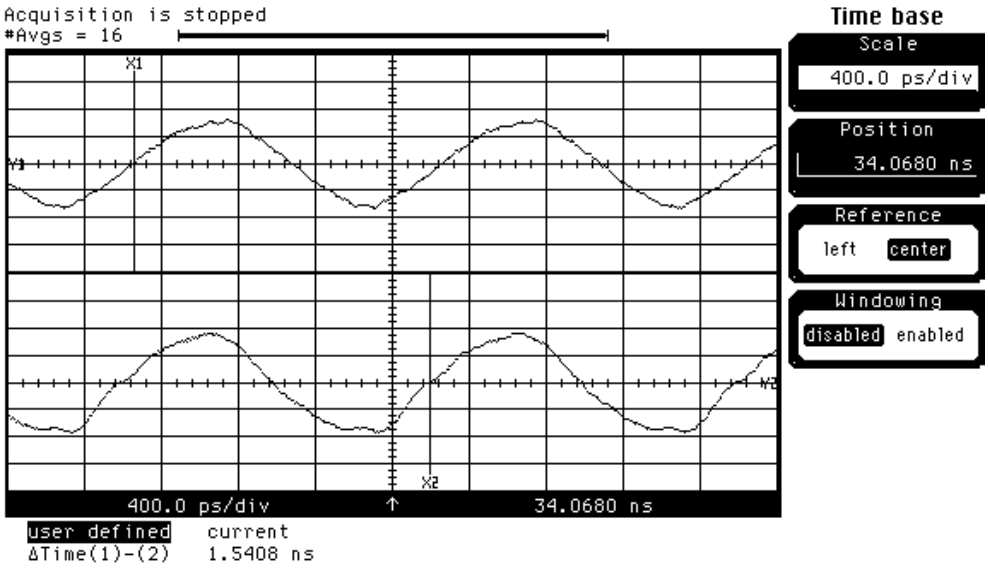
a Using oscilloscope channel 2, probe the J-clock signal on the underside of the stimulus board.

b In the oscilloscope Timebase menu, set the scale to 400 ps/div.

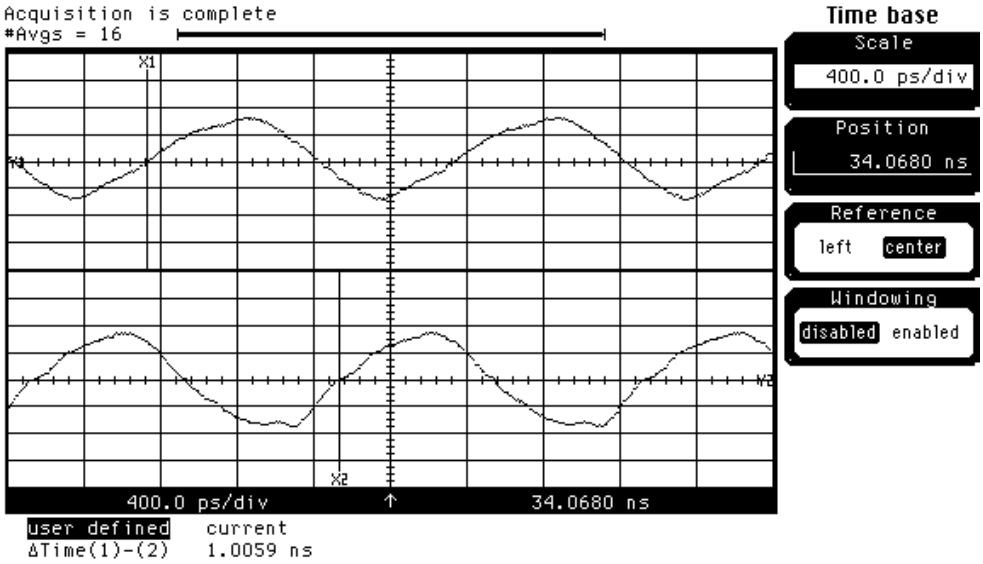
c Adjust the oscilloscope Timebase: Position until a rising edge appears within the second horizontal division from the left of the display.

d On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the delay.

e Using oscilloscope channel 1, probe data signal LD4 on the underside of the stimulus board.



f Adjust the pulse generator channel 1 Delay until the Δ Time(1)-(2) displays approximately 1.00 ns.



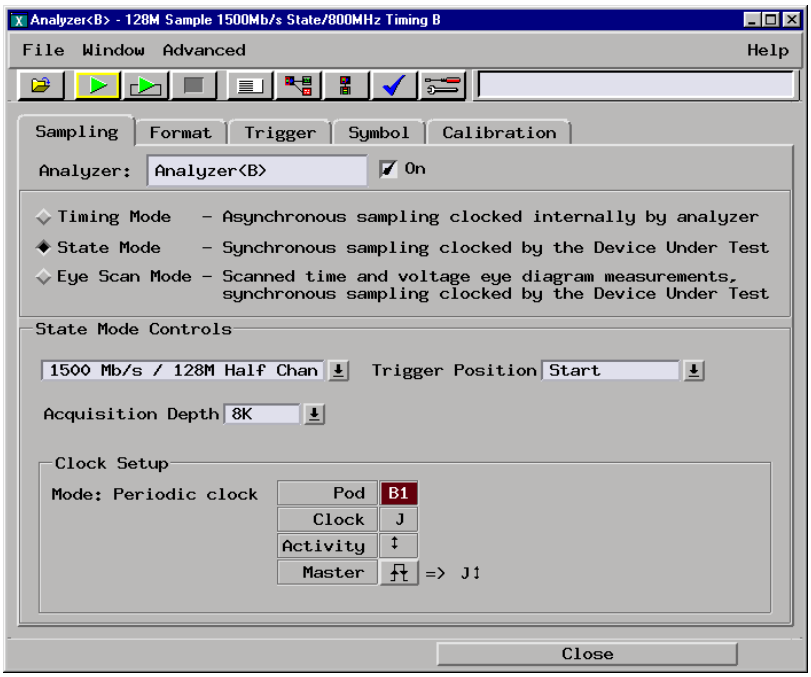
In this example, a value of -530 ps was entered for the pulse generator channel 1 Delay setting.

Set up the logic analyzer

1 Configure the logic analyzer acquisition.

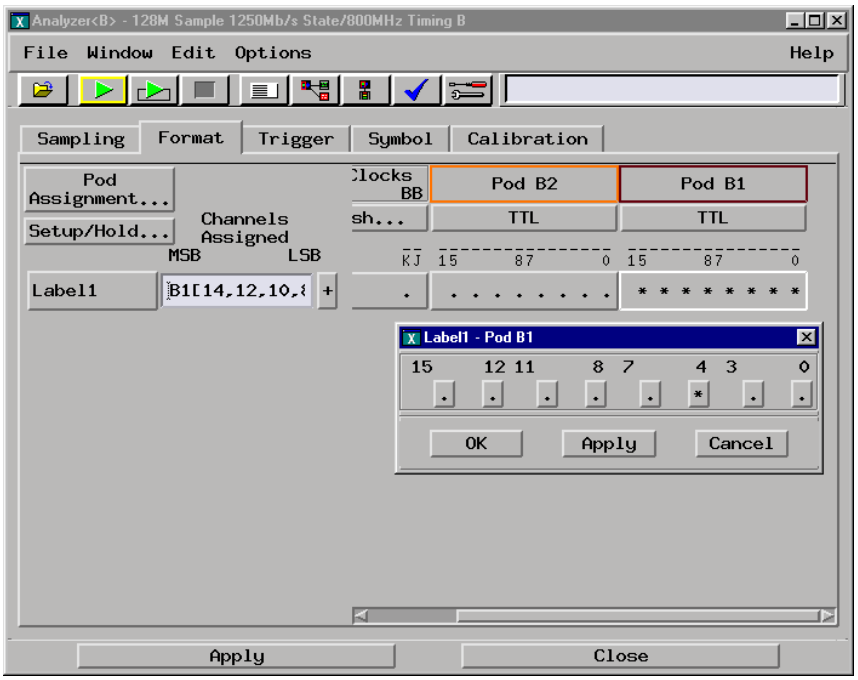
a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select the State Mode selection field, then select 1500 Mb/s / 128M Half Chan.



2 Configure the logic analyzer channels.

a Under the format tab, select the field showing the channel assignment for one of the pods being tested, then select Individual. Using the mouse, select channel 4.



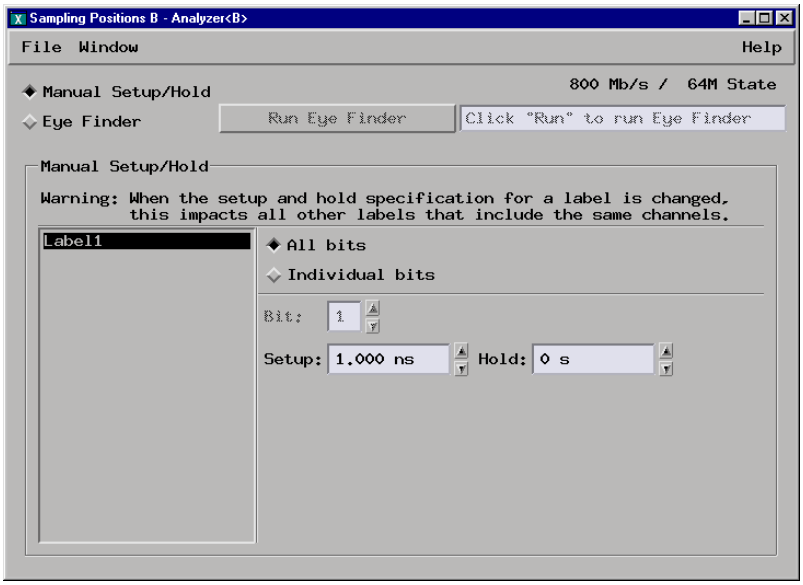
b Select OK to close the channel assignment window.

c Repeat a and b for the remaining pods to be tested.

d In the logic analyzer Setup and Trigger window, select the Format tab. Under the Format tab, select Setup/Hold... The Sampling Positions window will appear.

e In the Sampling Positions window, ensure All bits is selected.

f Enter a setup time of 1.000 ns then press the [Enter] key. The Hold: field should display “0 s”.



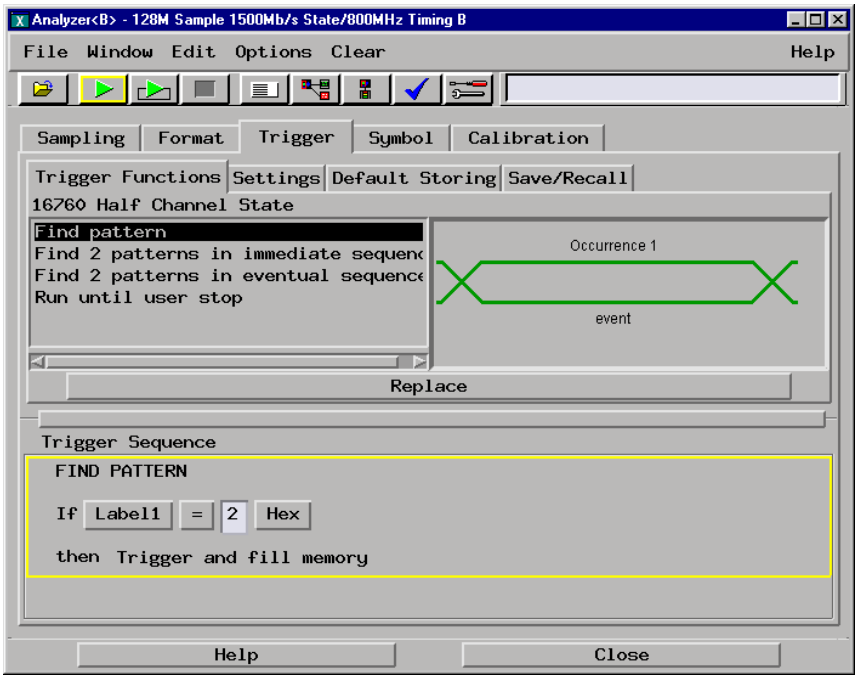
3 Configure the Trigger pattern.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger Functions tab, ensure the Find pattern trigger function is selected. If not, click Find pattern, then select Replace.

c If the trigger function reads If Anything, do the following steps: select Anything, then select Replace Event. At the pop-up, select Label. At the Label pop-up window, select Label1, then select OK.

d Under the Trigger Sequence, locate the Label = trigger pattern field. Enter “2” in the trigger pattern field. The trigger function should now read If Label1 = 2 Hex then Trigger and fill memory.



4 Verify the test data.

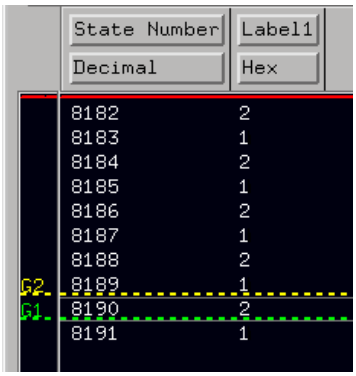
a In the Listing window, select the Run icon.

b In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the pattern field, enter "2". Select Apply, then select Close.

c In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the pattern field, enter "1". Select Apply, then select Close.

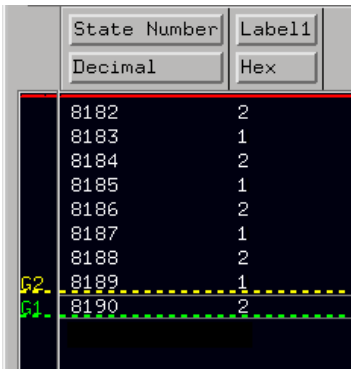
A PASS is determined by the markers counting the number of correct states. However, because the acquisition is prone to one prestore state, the Marker Setup window is configured to monitor the first state and the G2 marker is configured to count one less occurrence of the data "1".

With no prestore state, the Listing window will show:



and the Data at field in the Marker Setup window will show 2 as the data in the first stored state, the trigger state.

With one prestore state, the Listing window will show:



and the Data at field in the Marker Setup window will show 1 as the date in the first stored state, the prestore state.

Either of the above results passes the test.

Test passes if no error messages appear and the test data appears as explained above. If an error message appears, refer to Validating state mode test failures.

To test the high byte

Repeat the previous procedures substituting channel 12 for channel 4. Begin with “Characterize the stimulus board delay” on page 83 if necessary. If the stimulus board delay has already been characterized, enter the value in the pulse generator channel 1 delay and begin with “Set up the logic analyzer” on page 86.

To Test the Time Interval Accuracy

Testing the time interval accuracy does not check a specification, but does check the following:

- 125 MHz oscillator

This test verifies that the 125-MHz timing acquisition synchronizing oscillator on the logic analysis mainframe is operating within limits.

Equipment Required

Equipment	Critical Specifications	Recommended HP/Agilent Model/Part
Pulse Generator	750 MHz < 600 ps rise time	8133A Option 003
Function Generator	Accuracy ≤ (5)(10^{-6}) x frequency	8656B Option 002
SMA Coax Cable	18 GHz Bandwidth	8120-4948
BNC Cable		8120-1840
Adapter	SMA(m)-BNC(f)	1250-1200
Stimulus Board	no substitute	16760-60001

Set up the equipment

1 If you have not already done so, do the following procedures:

- "To Set up the Test Equipment and the Analyzer" on page 35
- "Characterize the stimulus board output threshold" on page 52

2 Activate the stimulus board.

a Plug in the stimulus power supply into line power. The green LED DS1 should illuminate showing that the stimulus board is active.

b On the stimulus board, press the Resynch VCO button.

3 Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Trigger
Mode: Ext	Mode: Square ÷ 1 Delay: 0.000 ns Ampl: 0.80 V Offs: 2.00 V COMP: Disabled (LED Off)	Divide: Divide ÷ 2 Ampl: 0.50 V Offs: 0.00 V

4 Set up the function generator according to the following table.

Function Generator Setup

Freq: 80.000 00 MHz	Amptd: 1.00 V	Modulation: Off

5 Activate the pulse generator Channel 2 OUTPUT.

Set up the logic analysis system

1 Set up the logic analysis session.

a Open a Session Manager window and select Start Session.

b In the Logic Analysis System window, select the module icon, then select Setup and Trigger. A Setup and Trigger window opens.

2 Configure the Sampling tab.

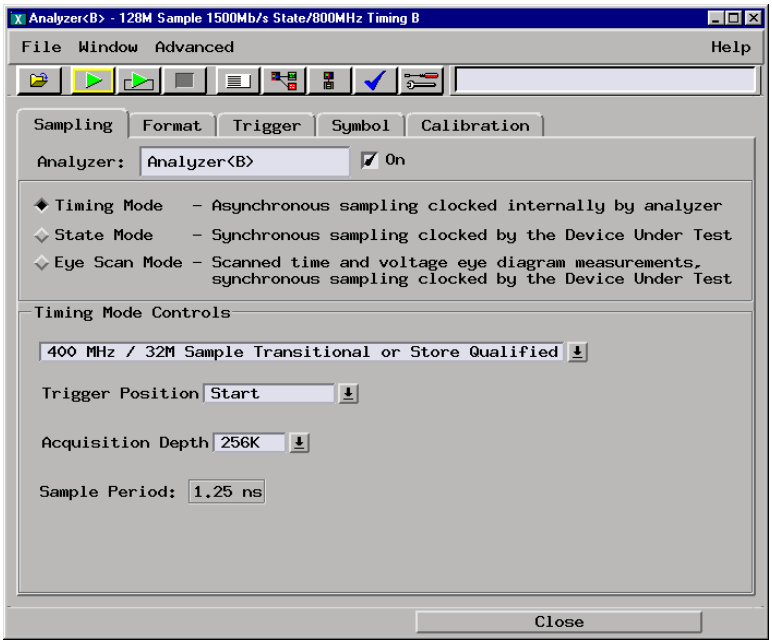
a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select Timing Mode.

c In the Timing Mode Controls, select the acquisition mode field, then select “400 MHz/32 M Sample Transitional or Store Qualified.”

d Select Trigger Position, then select Start.

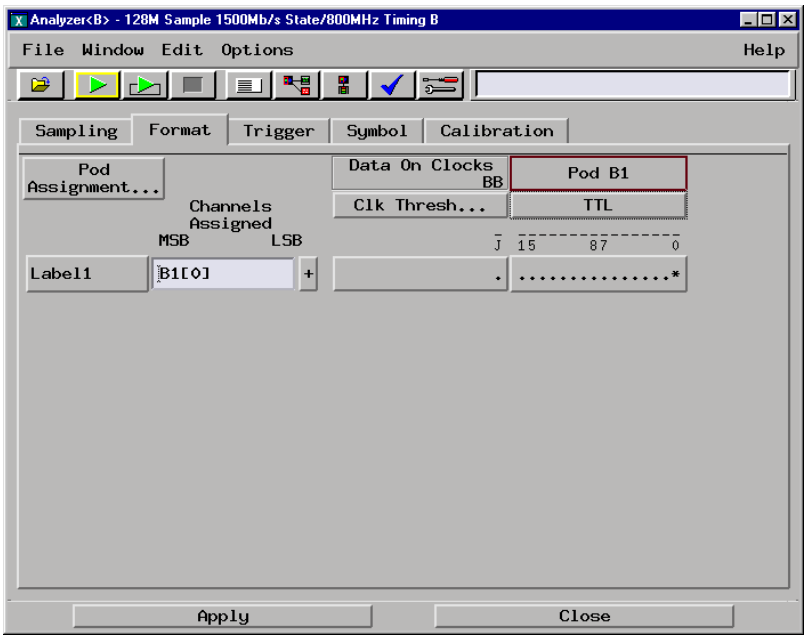
e Select the Acquisition Depth field, then select "256K."



3 Configure the Format tab.

a In the logic analyzer Setup and Trigger window, select the Format tab.

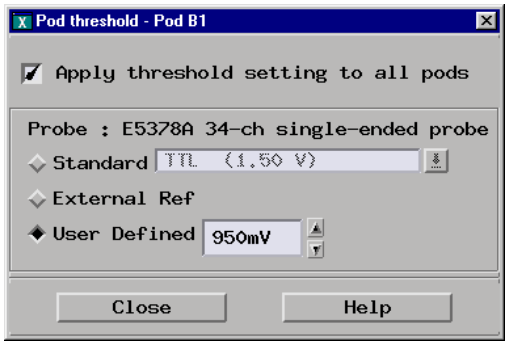
b Under the Format tab, select the field showing the channel assignment for Pod 1, then select Individual. Using the mouse, clear the channels (all "."), then select channel 0. An asterisk means that the channel is turned on.



c Select OK to close the channel assignment window.

d Under the Pod 1 field, select the threshold field. The Pod threshold window will appear.

e In the Pod threshold window, select User Defined, then select the threshold voltage field. Enter the V_{thresh} value you wrote in step 2e of Characterize the stimulus board output threshold.



f Select Close to close the Pod threshold window.

Pod 1 should now show activity.

4 Configure the Waveform window.

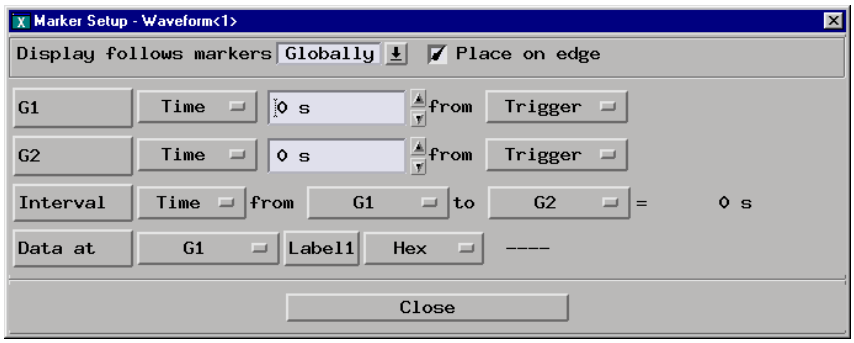
a In the Setup and Trigger window, select Window, then select Slot<n>: Analyzer<n> (where n is the slot the module under test is installed).

b At the pop-up menu. select Waveform. The Waveform window will appear.

c In the Waveform window, select the Marker tab.

d Select the G1 field and a Marker Setup window appears.

e Ensure that the Interval Time field reads “from G1 to G2” (instead of “from G2 to G1”).



Leave this window open as you will be using it later when acquiring data.

Acquire the data

1 Enable the pulse generator channel 2 and trigger outputs (with the LED off).

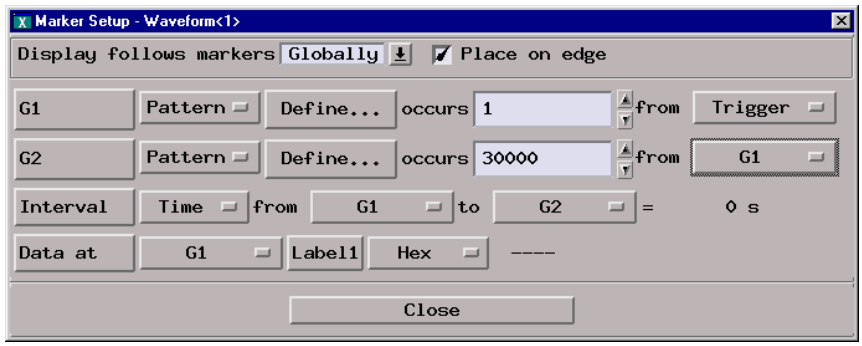
2 In the logic analyzer Waveform window, select Run.

3 Configure the Markers to measure the time interval.

a In the Marker Setup window select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.

b Select the Occurs field associated with G1 and enter “1”. Select the Occurs field associated with G2 and enter “30000”.

c Select the From field associated with G2 and select G1.



In the Marker Setup Window, you will observe the Interval Time from G1 to G2=value to determine the pass or fail status of this test.

d In the marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the Pattern field, enter “1”.

Select the Pattern Qualify field and select When Entering.

In the Marker Pattern window, select Apply, then select Close.

e In the marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the Pattern field, enter “1”.

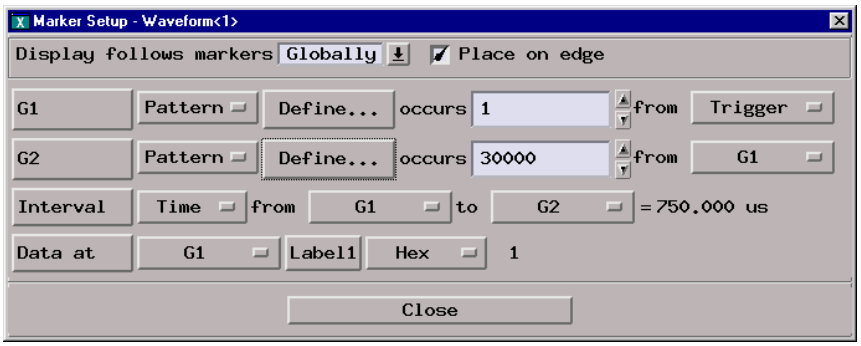
Select the Pattern Qualify field and select When Entering.

In the Marker Pattern window, select Apply, then select Close.

4 Acquire the data.

a Select the Run Repetitive icon. The logic analyzer repetitively acquires data.

b Continuously observe the Interval Time from G1 to G2=value in the Marker Setup window.



Allow the logic analyzer to run repetitively for approximately one minute. If the Interval Time value remains inside the range 749.921 µs to 750.079 µs, the test passes. Record a Pass or Fail in the performance test record.

c Select Stop to end the acquisition.

To Test the Multi-Card Module

Set up the equipment

If you have not already done so, do the procedure "Set up the equipment" on page 35. Ensure that the pulse generator is set up according to the tables in that section. Under the procedure "Connect the logic analyzer" on page 37, only steps 1 and 2 are necessary. Lastly, do the procedure "Characterize the stimulus board output threshold" on page 52.

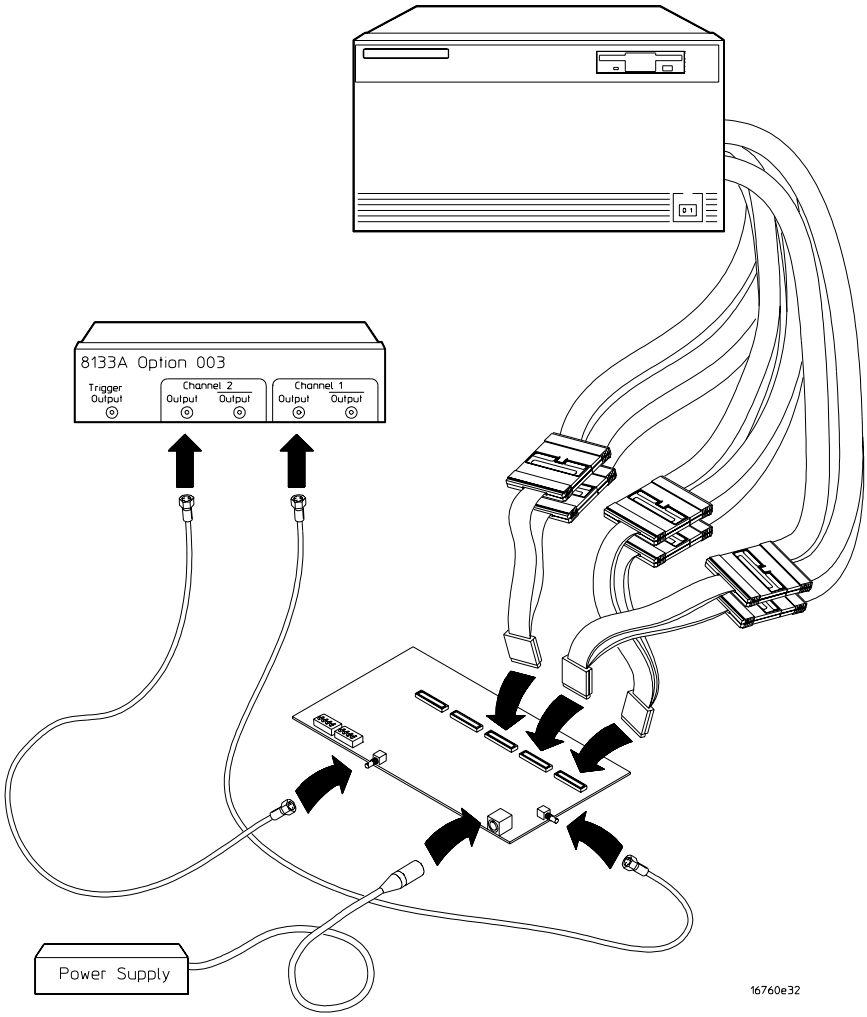
1 Connect the multicard module to the stimulus board.

a Connect an E5378A 100-pin single-ended probe to the master board. Connect the master board Pod 1 to the high density probe output marked "Odd." Connect the master board Pod 2 to the high density probe output marked "Even."

b Connect the probe input to stimulus board connector Pod 5.

c Repeat step a for the top-most expander card. Then connect the probe input for the top-most card to stimulus board connector J4.

d For a three-, four-, or five- card module, repeat step a for the bottom-most expander card. Then connect the probe input for the bottom most card to stimulus board connector J3.



2 Set up the pulse generator.

Enter the delay value for LD4 from “Characterize the stimulus board delay” on page 83 into the pulse generator channel 1 delay.

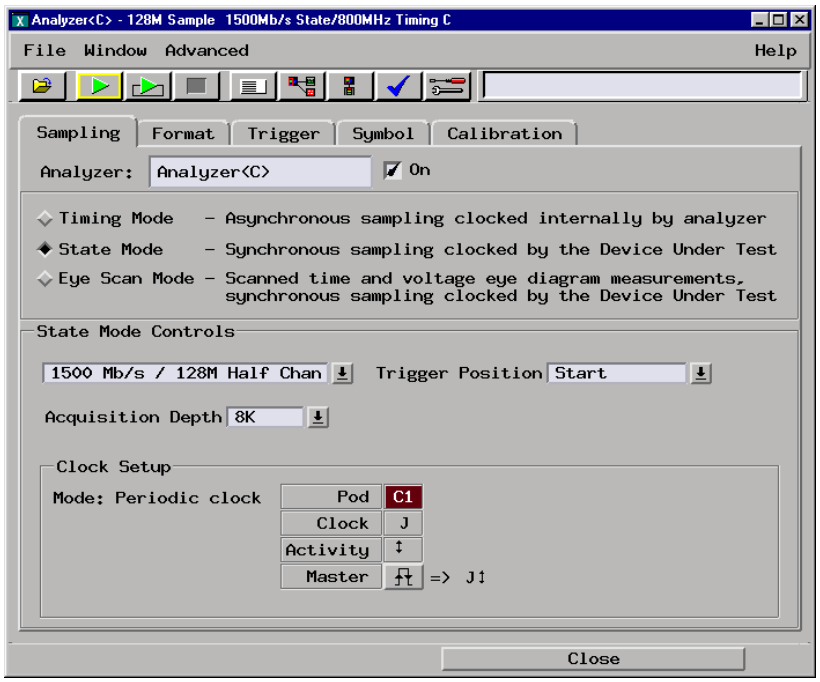
Set up the logic analyzer

1 Configure the Sampling tab.

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select State Mode.

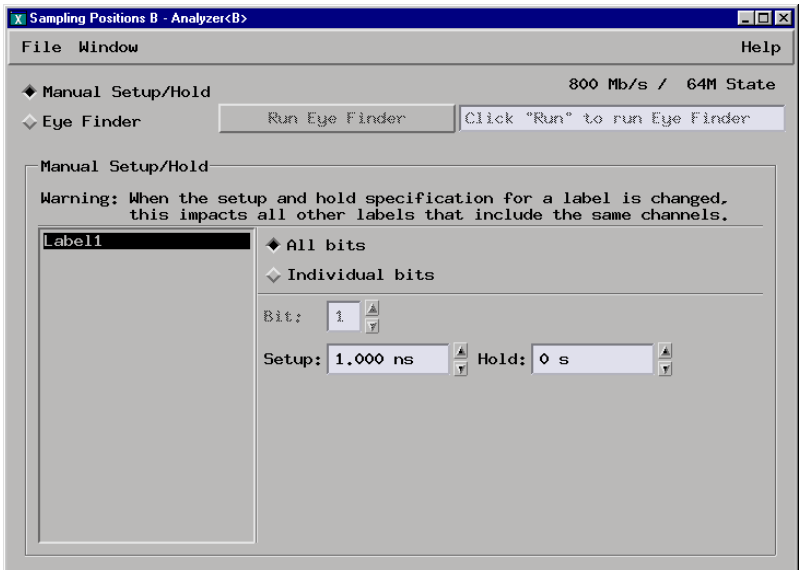
c Select the State Mode selection field, then select 1500 Mb/s / 128 M Half Chan.



d In the logic analyzer Setup and Trigger window, select the Format tab. Under the Format tab, select Setup/Hold... The Sampling Positions window will appear.

e In the Sampling Positions window, ensure All bits is selected.

f Enter a setup time of 1.000 ns then press the [Enter] key. The Hold: field should display “0 s”.



2 Configure the Trigger settings.

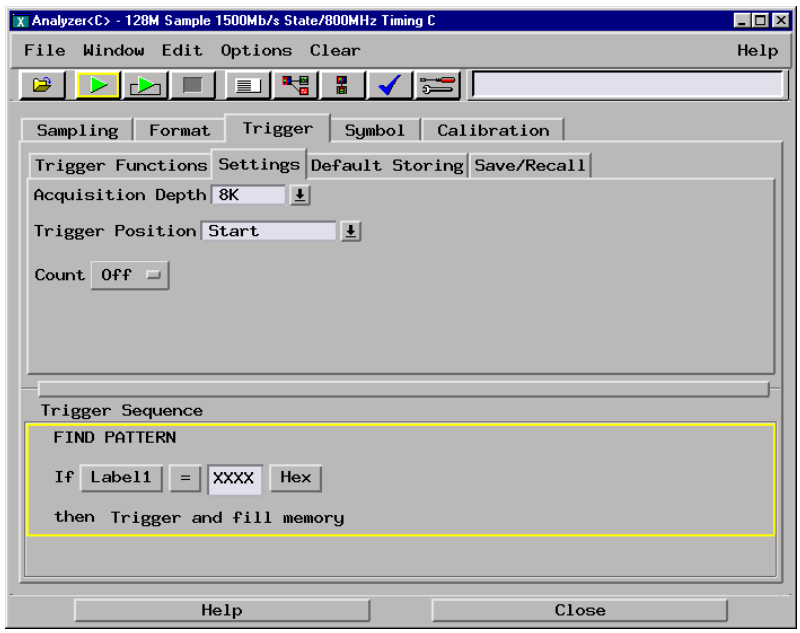
a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger tab, select the Settings tab.

c Select the Acquisition Depth field, then select 8K.

d Select the Trigger Position field, then select Start.

e Select the Count field, then select Off.

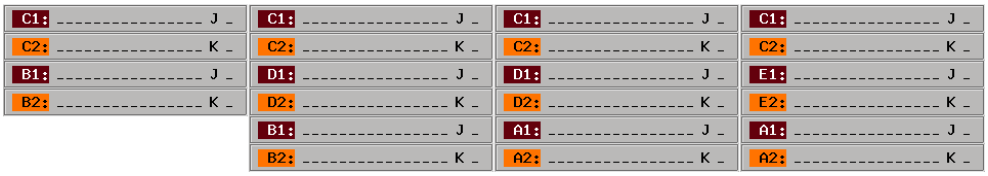


3 Configure the Format tab pod and channel assignments.

a In the logic analyzer Setup and Trigger window, select the Format tab.

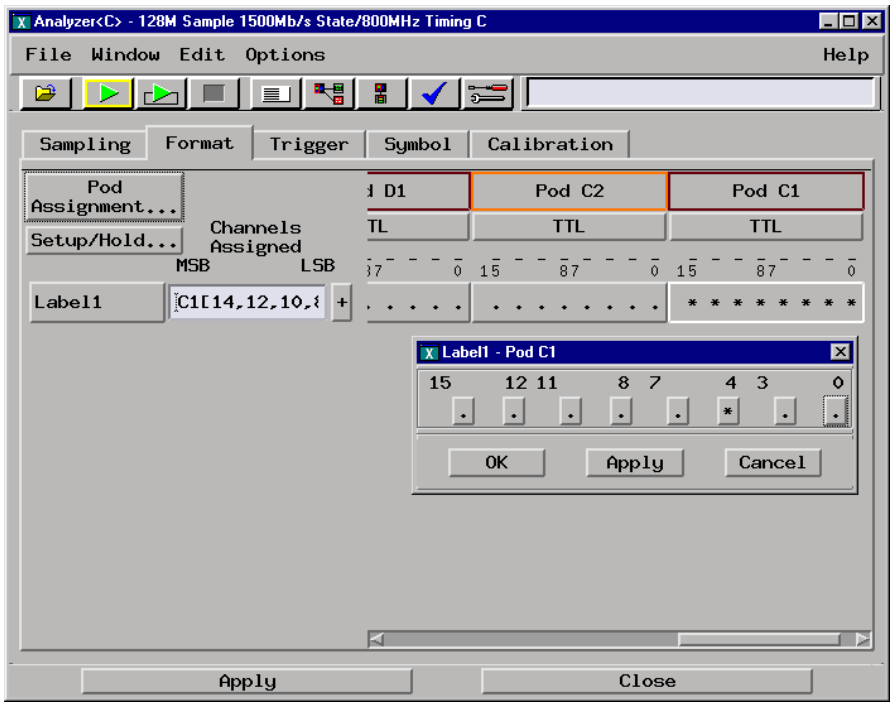
b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag the pods for the master card, top-most expander card, and bottom-most expander card (if present) to the Analyzer 1 column. The possible configurations look like this (master card is in slot C):



d Select Close to close the Pod Assignment window.

e Under the Format tab, select the field showing the channel assignments for one of the pods being tested, then select Individual. Using the mouse, select channel 4 of each pod. An asterisk (*) means that a channel is turned on.



f Select OK to close the channel assignment window.

g Repeat e and f for all pods.

4 Reconfigure the logic analyzer thresholds to the output threshold levels.

a Under the Format tab, select the threshold field under either pod. The Pod threshold window will appear.

b In the Pod threshold window, ensure Apply threshold setting to all pods is checked.

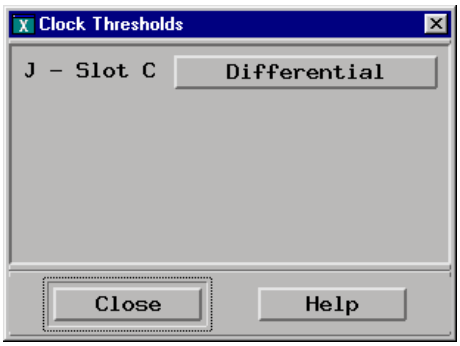
c In the Pod threshold window, select User Defined, then select the threshold voltage field. Enter the V_{thresh} value you wrote in setup 2 e of Characterize the demo board output threshold.

d Select Close to close the Pod threshold window.

e Under the Format tab, select the Clk Thresh... field. The Clock threshold window will appear.

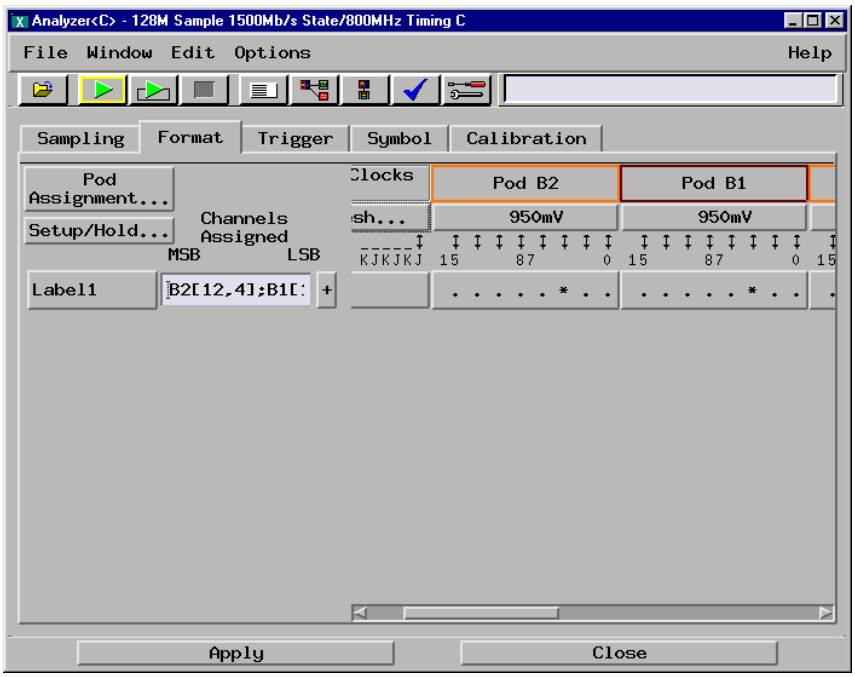
f Select the threshold field associated with J-clock. The J threshold window will appear.

g In the J threshold window, select Differential.



h Select Close to close the J threshold window, then select Close to close the Clock threshold window.

The pods and J-clock should now show activity.



Verify the test data

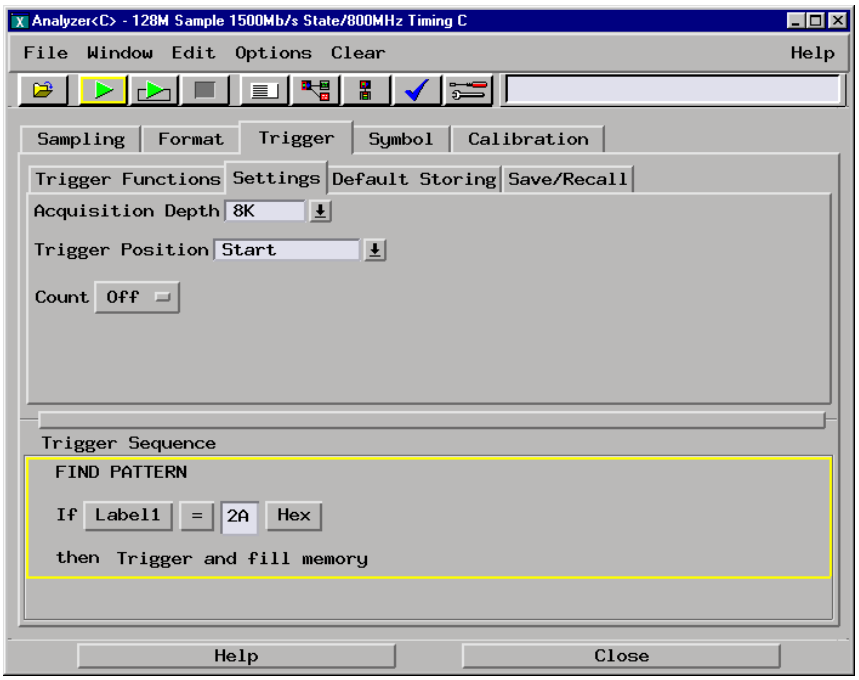
1 Configure the Trigger pattern.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger Functions tab, ensure the Find pattern trigger function is selected. If not, click Find pattern, then select Replace.

c If the trigger function reads If Anything, do the following steps: select Anything, then select Replace Event. At the pop-up, select Label. At the Label pop-up window select Label1, then select OK.

d Under Trigger Sequence, locate the Label1 = trigger pattern field. Enter "2A" ("A" for a two-card module) in the trigger pattern field. The trigger function should now read If Label1 = 2A Hex then Trigger and fill memory.



2 Configure the Listing window.

a In the Setup and Trigger window, select Window, then select Slot<n>: Analyzer<n> (where n is the slot the master card test is installed). At the pop-up menu, select Listing. The Listing window will appear.

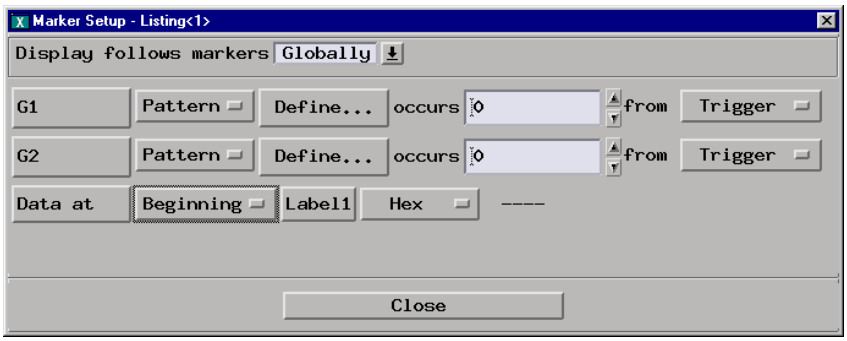
b In the Listing window, select the Markers tab.

c Select the G1: field and the Markers Setup window appears.

d Select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.

e Right click over the Interval field, then select Delete.

f Select the Trigger field associated with Data at and select Beginning.



NOTE: Leave the Marker Setup window open. You will be entering numeric values in the "occurs" field after acquiring the test data.

3 In the Listing window, select the Run icon.

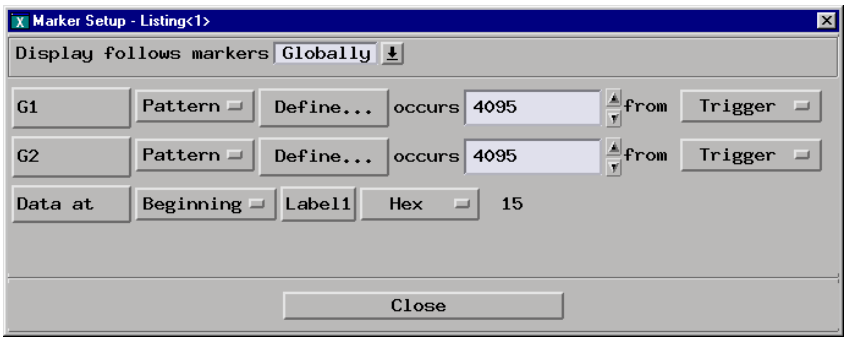
4 Configure the markers.

a In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the pattern field, enter "2A" ("A" for a two-card module). Select Apply, then select Close.

b In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Patern window appears. In the pattern field, enter "15" ("5" for a two-card module). Select Apply, then select Close.

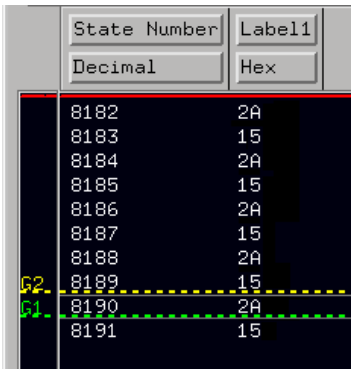
c In the Marker Setup window, select the 'occurs' value field that corresponds to marker G1. Enter 4095.

d In the Maker Setup window, select the 'occurs' value field that corresponds to marker G2. Enter 4095.



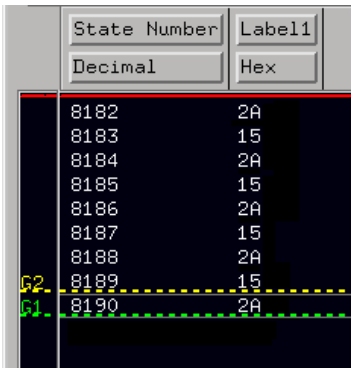
A PASS is determined by the markers counting the number of correct states. However, because the acquisition is prone to one prestore state, the Marker Setup window is configured to monitor the first state and the G2 marker is configure to count one less occurrence of the data “15” (“5” for a two-card module).

With no prestore state, the Listing window for a three-, four-, or five-card module will show:



The Data at field in the Marker Setup window for a three-, four-, or five-card module will show “2A” as the data in the first stored state, the trigger state.

With one prestore state, the Listing window for a three-, four-, or five-card module will show:



The Data at field in the Marker Setup window for a three-, four-, or five card module will show “15” as the data in the first stored state, the prestore state.

Either of the above results passes the test.

Performance Test Record

Performance Test Record

	16760A Logic Analyzer
Serial No. _____	Work Order No._____
Recommended Test Interval - 2 Year/4000 hours	Date_____
Recommended next testing_____	Temperature_____

Test	**Settings**	**Results**
Self-Tests		Pass/Fail _____
Threshold Accuracy	±(30 mV + 1.0% of threshold setting)	Pass/Fail _____
200 Mb/s State Acquisition Mode		
State Acquisition Speed		Pass/Fail _____
Double-edge Clock Setup Time		Pass/Fail _____
Single-edge Clock Setup Time		Pass/Fail _____
Single-edge Clock Hold Time		Pass/Fail _____
400 Mb/s State Acquisition Mode		
State Acquisition Speed		Pass/Fail _____
Double-edge Clock Setup Time		Pass/Fail _____
Single-edge Clock Setup Time		Pass/Fail _____
Single-edge Clock Hold Time		Pass/Fail _____
800 Mb/s State Acquisition Mode		
State Acquisition Speed		Pass/Fail _____
Double-edge Clock Setup Time		Pass/Fail _____
Single-edge Clock Setup Time		Pass/Fail _____
Single-edge Clock Hold Time		Pass/Fail _____
1500 Mb/s State Acquisition Mode		
State Acquisition Speed		Pass/Fail _____
Time Interval Accuracy		Pass/Fail _____
Multi-card Test		
State Acquisition		Pass/Fail _____

4

Calibrating

This chapter gives you instructions for calibrating the logic analyzer.

Calibration Strategy

The 16760A logic analyzer does not require an operational accuracy calibration. To test the module against the module specifications, refer to "Testing Performance" in chapter 3.

5

Troubleshooting

This chapter helps you troubleshoot the module to find defective assemblies.

The troubleshooting consists of flowcharts, self-test instructions, a cable test, and a test for the auxiliary power supplied by the probe cable.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform the self-tests or the cable test.

The service strategy for this instrument is the replacement of defective assemblies. This module can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

CAUTION: Electrostatic discharge can damage electronic components. Use grounded wrist-straps and mats when you perform any service to this instrument or to the cards in it.

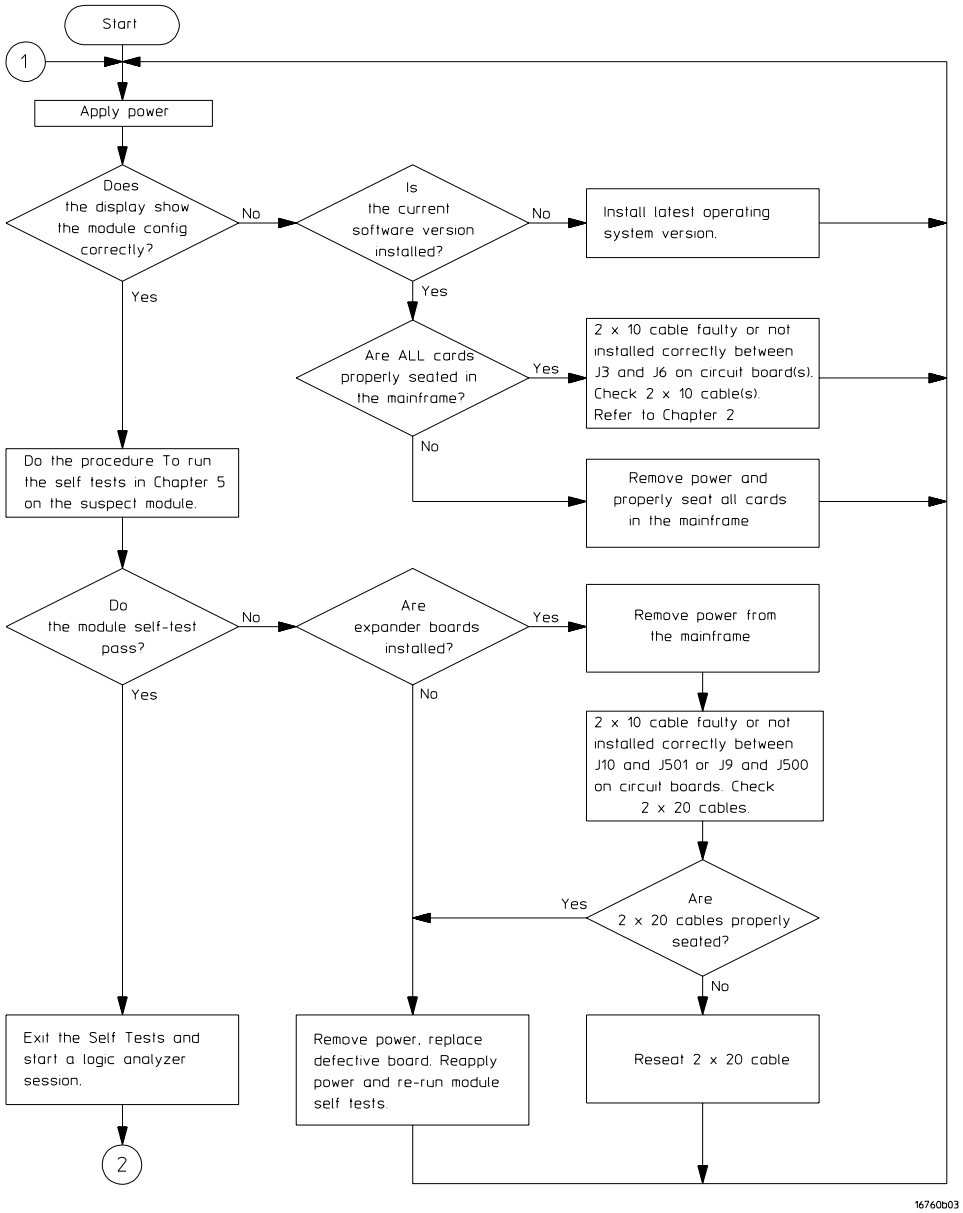
To use the flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled numbers on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart.

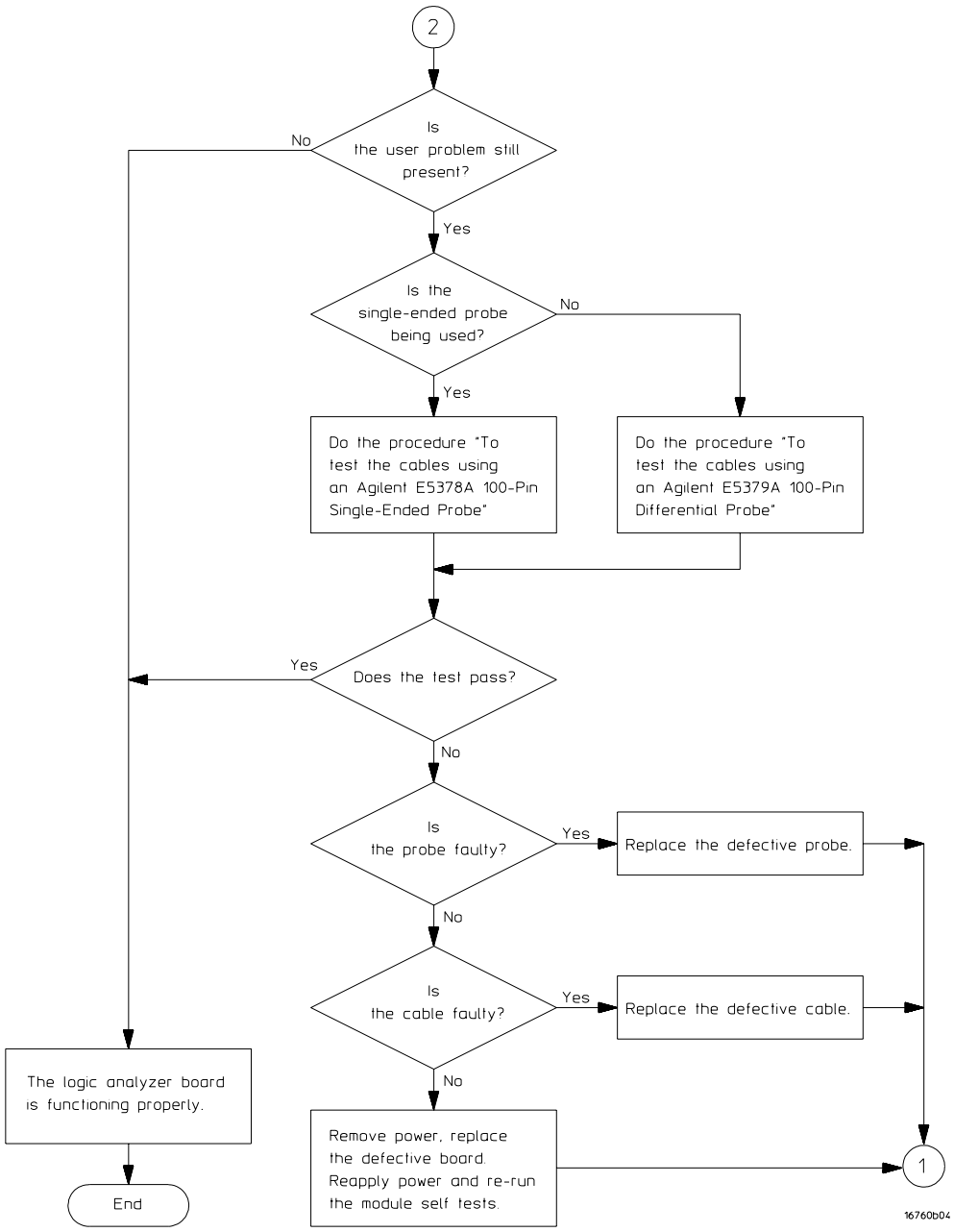
Mainframe Operating System

Before starting the troubleshooting on an 16760A, ensure that the required version of Agilent Technologies 16700 -series mainframe operating system is installed on the mainframe. The required operating system software versions are listed in “Mainframe and Operating System” on page 10. To check the operating system version number, open the System Administration window, click the Admin tab, then click About...

If the proper version is not loaded, obtain a copy of the updated operating system software and install it in the logic analyzer.



Troubleshooting Flowchart 1



Troubleshooting Flowchart 2

To run the self-tests

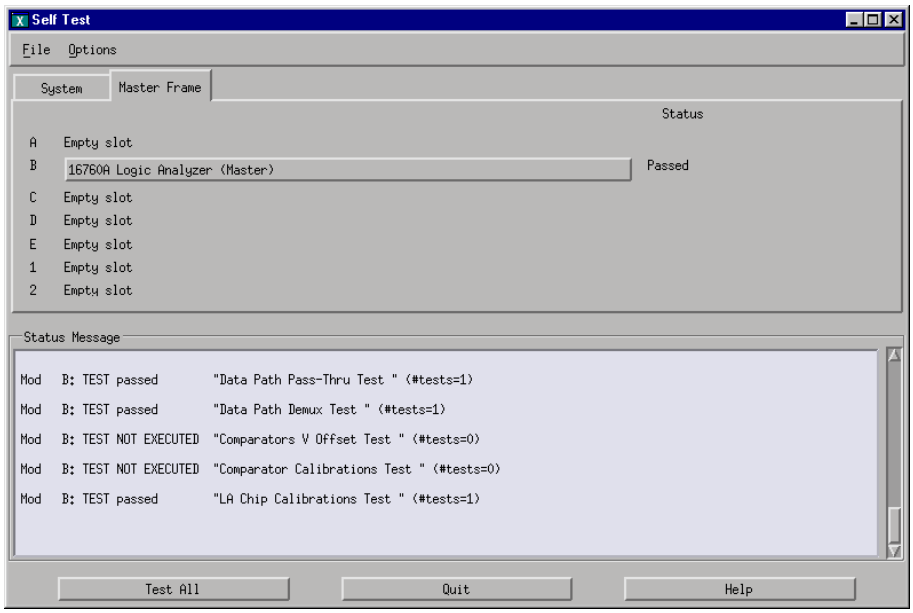
Self-tests identify the correct operation of major, functional subsystems of the module. You can run all self-tests without accessing the module. If a self-test fails, the troubleshooting flowcharts instruct you to change a part of the module.

To run the self-tests:

1. In the System window, select the System Administration icon.
2. In the System Administration window, select the Admin tab, then select Self-Test. At the Test Query window, select Yes.

   The tests can be run individually, or all the tests can be run by selecting Test All at the bottom of the Self Test window. Note that if Test All is selected, system tests requiring user action will not be run. For more information, refer to Chapter 8 in the mainframe service manual.
3. In the Self Test window under the System tab, select System CPU Board.
4. Run the floppy drive test.
   a. In the Self Test: System CPU Board window, select Floppy Drive Test.
   b. Insert a DOS-formatted disk with 300KB of available space in the mainframe floppy drive.
   c. In the Test Query window, select OK.

      The Test Query window instructs you to insert the disk into the disk drive. The other System CPU Board tests require similar user action to successfully run the test.
5. In the Self Test: System CPU Board window, select Close to close the window.
6. In the Self Test window, select PCI Board. Select Test All to run all PCI board tests.
7. In the Self Test window, select the Master Frame tab. Select the 16760A module to be tested, then select Test All to run all the module tests. The module test status should indicate PASSED (see screen on next page).



Refer to Chapter 8 in the mainframe service manual for more information on system tests that are not executed.

To exit the test system

To exit the test system

1. Select Close to close any module or system test windows.
2. In the Self Test window, select Quit.
3. In the session manager window, select Start Session to launch a new logic analyzer session.

To test the cables using an Agilent E5378A Probe

This test allows you to functionally verify the logic analyzer cable and an Agilent E5378A probe.

Equipment Required

Equipment	Critical Specification	Recommended Part
Stimulus Board	No Substitute	16760-60001

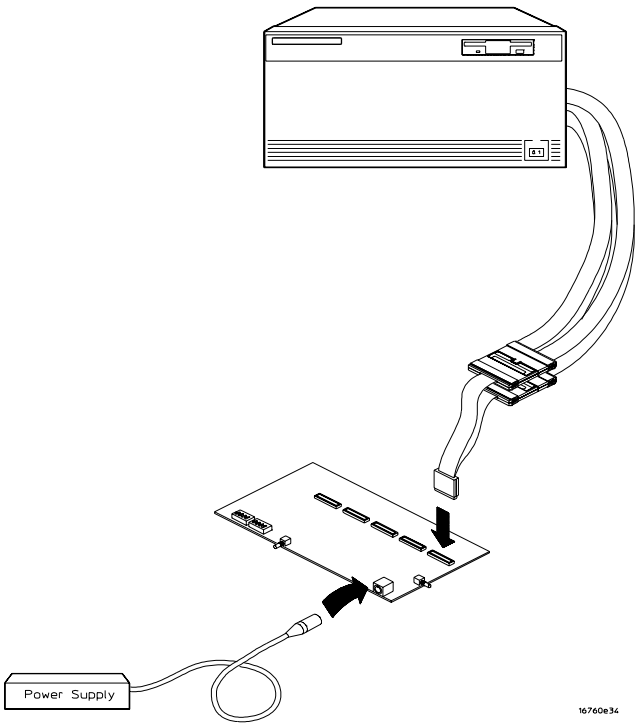
1 Connect the logic analyzer to the stimulus board.

a Connect an Agilent E5378A 100-pin single-ended probe to the logic analyzer module. Connect logic analyzer Pod 1 to the probe output marked “Odd.” Connect logic analyzer Pod 2 to the probe output marked “Even.”

b Connect the probe input to stimulus board connector Pod 1.

c Connect a power cord to the stimulus board power supply. Connect the stimulus board power supply output to the stimulus board power supply connector J82.

d Plug in the stimulus power supply into line power. The green LED DS1 should illuminate showing that the stimulus board is active



2 Set up the stimulus board.

a Configure the oscillator select switch S1 according to the following settings:

- S1 Off
- S2 Off
- S3 Off
- Int

b Configure the data mode switch S4 according to the following settings:

- Even
- Count

c Press the Resynch VCO button, then Counter RST (Counter Reset) button.

3 Set up the logic analyzer

a Open the Session Manager window and select “Start Session.”

b In the logic analyzer system window, select the module icon, then select Setup and Trigger. A Setup and Trigger window appears.

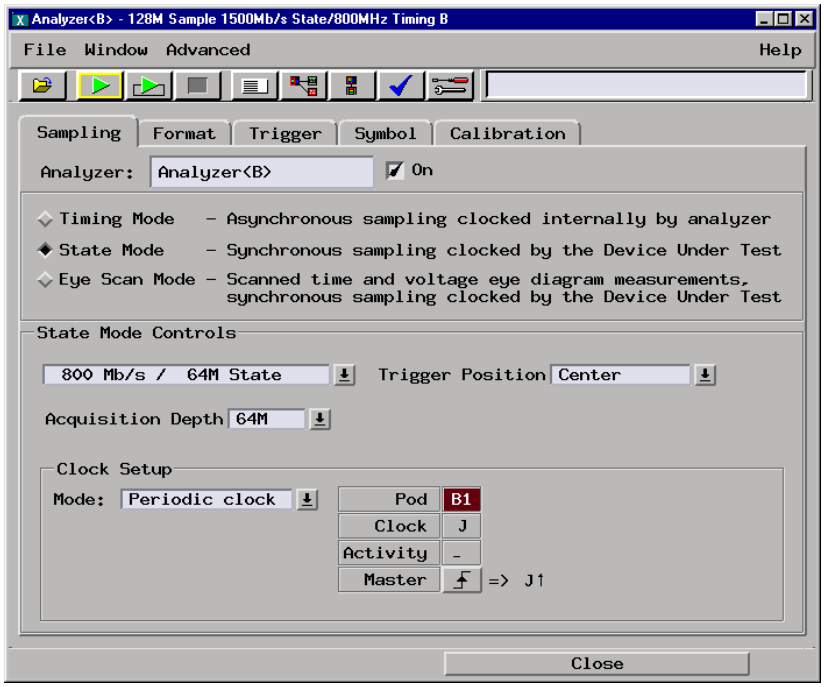
c In the logic analysis system window, select the module icon, then select Listing. A Listing window appears.

4 Set up the Sampling tab

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select State Mode.

c Select the clock edge field for J-clock, then select Rising Edge.



5 Configure the Trigger settings

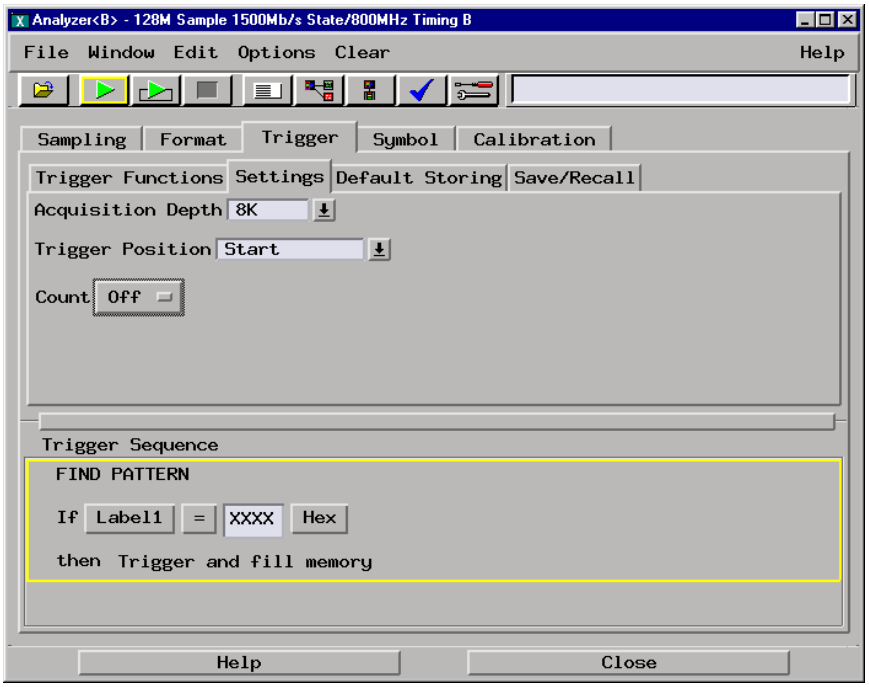
a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger tab, select the Settings tab.

c Select the Acquisition Depth field, then select 8K.

d Select the Trigger Position field, then select Start.

e Select the Count field, then select Off.

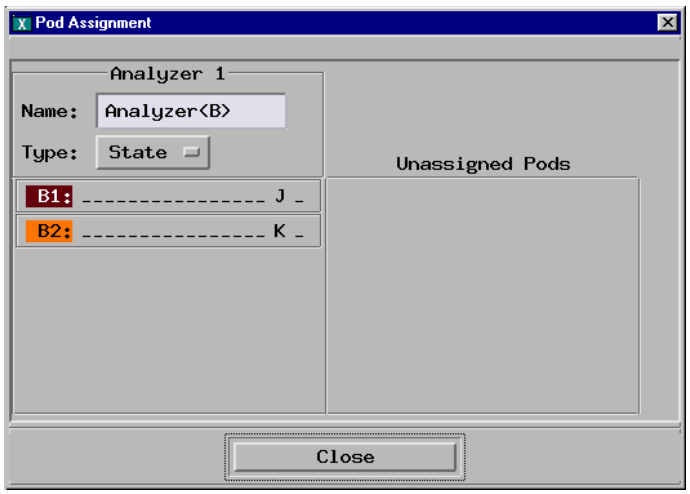


6 Configure the Format tab

a In the logic analyzer Setup and Trigger window, select the Format tab.

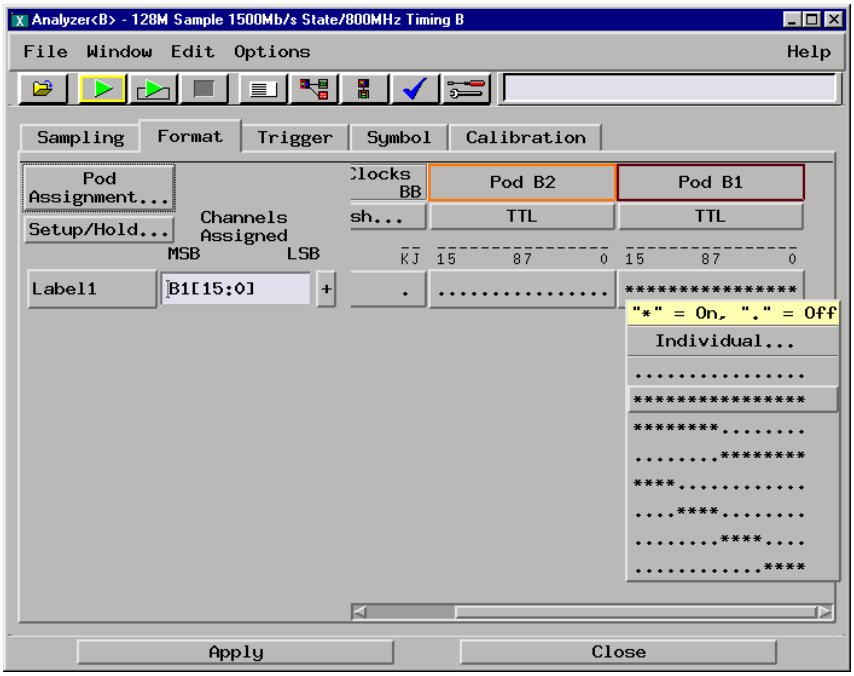
b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag the pods to the Analyzer 1 column.



d Select Close to close the pod assignment window.

e Under the Format tab, select the field showing the channel assignments for one of the pods being tested, then select "**********" to active all channels.



f Select OK to close the channel assignment window.

g Repeat e and f for the remaining pods to be tested.

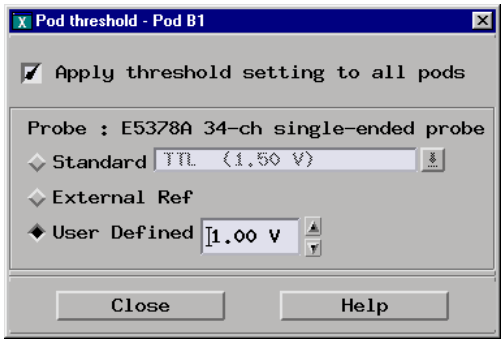
7 Configure the logic analyzer thresholds

a In the logic analyzer Setup and Trigger window, select the Format tab.

b Under the Format tab, select the threshold field under either pod. The Pod threshold window will appear.

c In the Pod threshold window, ensure the Apply threshold setting to all pods is checked.

d In the Pod threshold window, select User Defined, then select the threshold voltage field. Enter 1.00V.

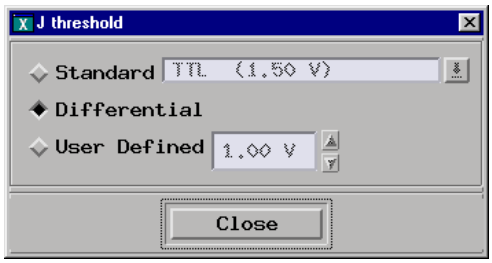


e Select Close to close the pod threshold window.

f Under the Format tab, select the Clk Thresh... field. The clock threshold window will appear.

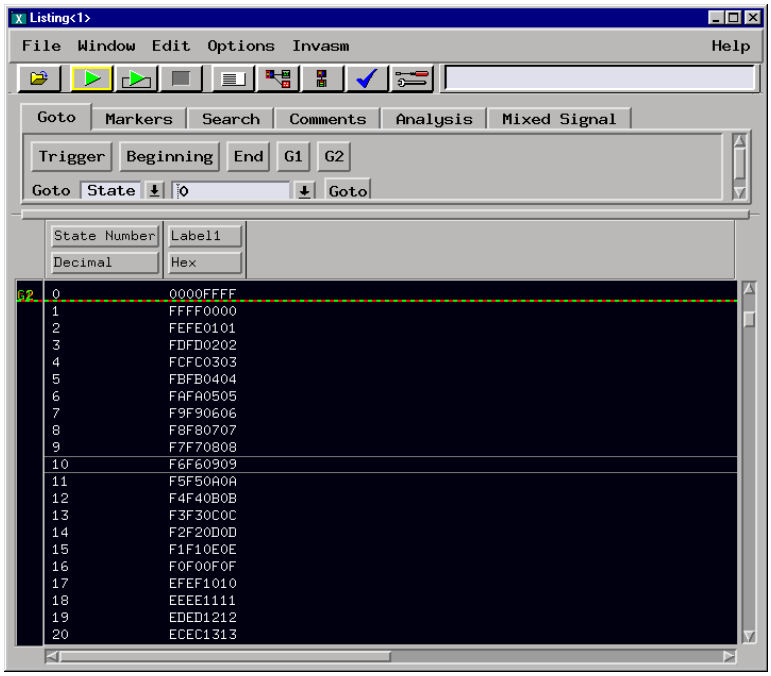
g Select the threshold field associated with J-clock. The J threshold window will appear.

h In the J threshold window, select Differential.



i Select Close to close the J threshold window, then select Close to close the Clock threshold window.

8 On the logic analyzer, select Run. The listing should look similar to the figure below.



Scroll down at least 256 states to verify the data. The lower two bytes (four digits) of Label1 show two incrementing binary counters. The upper two bytes of Label1 show two decrementing binary counters. If the listing does not look similar the figure, then there is a possible problem with the cable or high density adapter. Causes for cable test failure include:

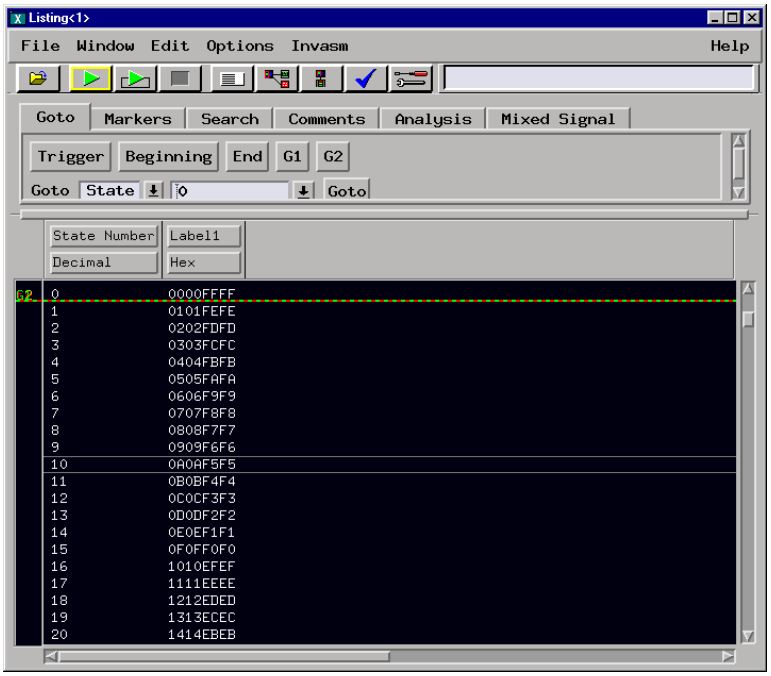
- open channel
- channel shorted to a neighboring channel
- channel shorted to either ground or a supply voltage

If the test data on either the lower two bytes or the upper two bytes is not correct, then perform the following step to isolate the failure.

9 Verify the failure

a Reconnect probe adapter to the logic analyzer module. Connect logic analyzer Pod 1 to the probe adapter output marked “Even.” Connect logic analyzer Pod 2 to the probe adapter output marked “Odd.”

b On the logic analyzer, select Run. Note the lower two bytes now displays two decrementing counters, the upper two bytes displays two incrementing counters.



If the error in the test data remains the same two bytes as the previous run (that is, the error follows the cable) then the cable is suspect.

If the error is now in the opposite two bytes (that is, the error follows the E5378A probe adapter) the probe adapter is suspect.

Return to the troubleshooting flowchart.

To test the cables using an Agilent E5379A Probe

This test allows you to functionally verify the logic analyzer cable and an Agilent E5379A probe.

Equipment Required

Equipment	Critical Specification	Recommended Part
Stimulus Board	No Substitute	16760-60001

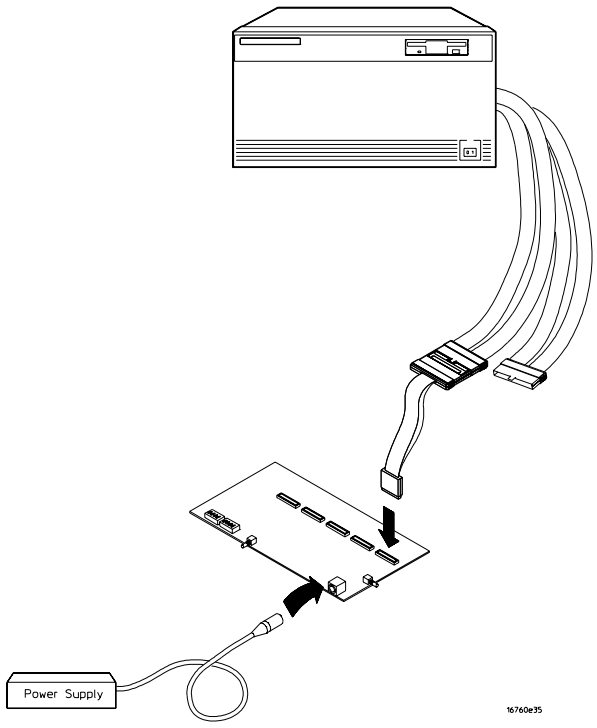
1 Connect the logic analyzer to the stimulus board.

a Connect an Agilent E5379A 100-pin differential probe to the logic analyzer cable to be tested.

b Connect the probe input to the stimulus board connector Pod 1.

c Connect a power cord to the stimulus board power supply. Connect the stimulus board power supply output to the stimulus board power supply connector J82.

d Plug in the stimulus power supply into line power. The green LED DS1 should illuminate showing that the stimulus board is active.



2 Set up the stimulus board

a Configure the oscillator select switch S1 according to the following settings:

- S1 Off
- S2 Off
- S3 Off
- Int

b Configure the data mode switch S4 according to the following settings:

- Even
- Count

c Press the Resynch VCO button, then the Counter RST (Counter Reset) button.

3 Set up the logic analyzer

a Open the Session Manager window and select “Start Session.”

b In the Logic Analysis System window, select the module icon, then select Setup and Trigger. A Setup and Trigger window appears.

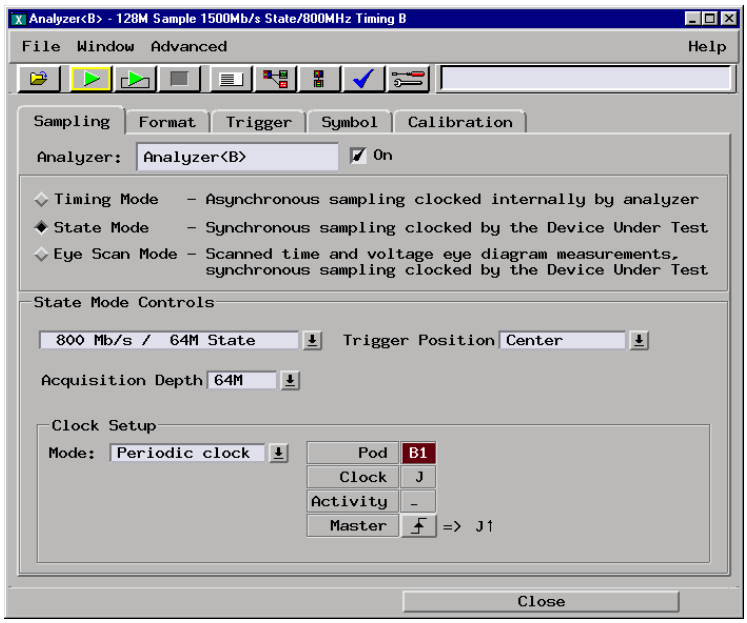
c In the Logic Analysis System window, select the module icon, then select Listing. A Listing window appears.

4 Set up the Sampling tab

a In the logic analyzer Setup and Trigger window, select the Sampling tab.

b Under the Sampling tab, select State Mode.

c Select the clock edge field for J-clock, then select Rising Edge.



5 Configure the Trigger settings

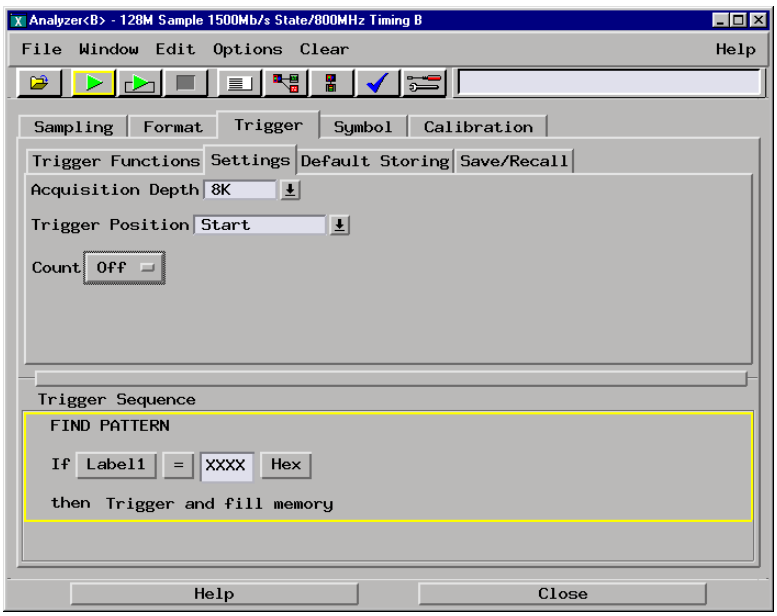
a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Under the Trigger tab, select the Settings tab.

c Select the Acquisition Depth field, then select 8K.

d Select the Trigger Position field, then select Start.

e Select the Count field, then select Off.

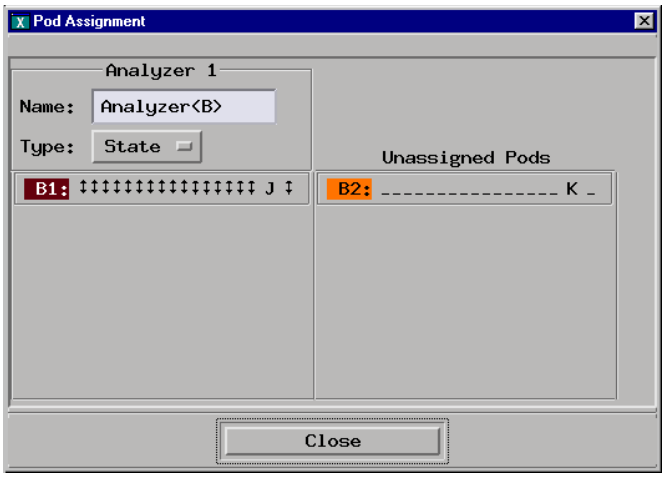


6 Configure the Format tab

a In the logic analyzer Setup and Trigger window, select the Format tab.

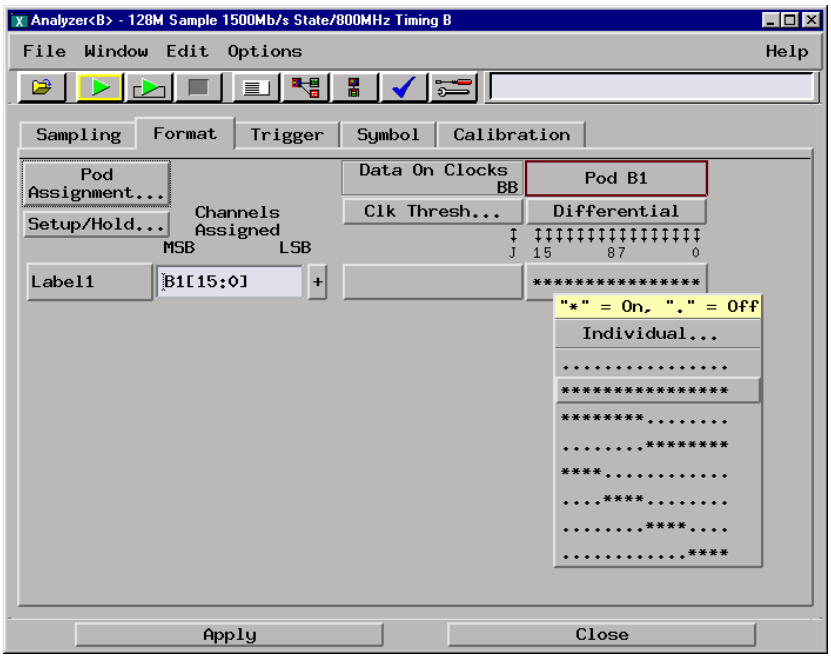
b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag the pod under test to the Analyzer 1 column.



d Select Close to close the pod assignment window.

e Under the Format tab, select the field showing the channel assignment for the pod under test, then select "**********" to activate all channels.



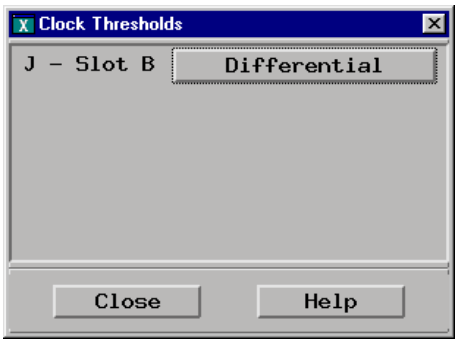
f Select OK to close the channel assignment window.

7 Configure the logic analyzer thresholds

a Under the Format tab, select the CLK Thresh... field. The Clock threshold window will appear.

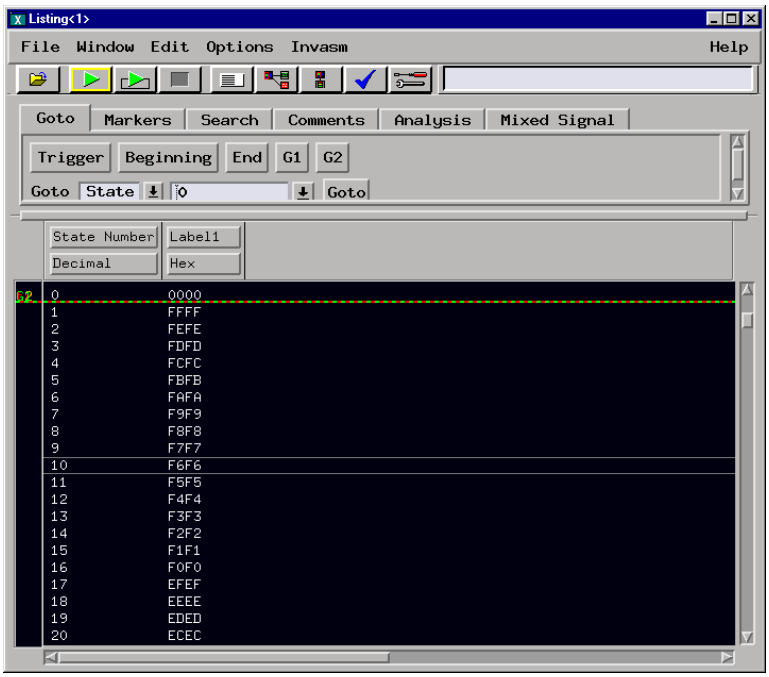
b Select the threshold field associated with J-clock. The J threshold window will appear.

c In the J threshold window, select Differential.



d Select Close to close the J threshold window, then select Close to close the Clock threshold window.

8 On the logic analyzer, select Run. The listing should look similar to the figure below.



Scroll down at least 256 states to verify the data. Label1 shows two decrementing binary counters. If the listing does not look similar to the figure, then there is a possible problem with the cable or high density probe adapter. Cause for cable test failures include:

- open channel
- channel shorted to a neighboring channel
- channel shorted to either ground or a supply voltage

If the test data is not correct, then perform the following step to isolate the failure.

9 Verify the failure

a Reconnect probe adapter to the other logic analyzer cable.

b Repeat step 6 through 8 to reconfigure the Format tab in the Setup and Trigger window. Deactivate the pod just tested. Activate the pod to be tested and assign all channels to Label1.

c On the logic analyzer, select Run. The expected test data is the same as in step 8 above.

If the test data is now correct (that is, the error follows the cable) then the cable is suspect.

If the test data is still not correct (that is, the error follows the E5379A probe adapter) the probe adapter is suspect.

Return to the troubleshooting flowchart.

6

Replacing Assemblies

This chapter contains the instructions for removing and replacing the logic analyzer module, the circuit board of the module, and the probe cables of the module as well as the instructions for returning assemblies.

CAUTION: Turn off the instrument before installing, removing, or replacing a module in the instrument.

Tools Required

- A T10 TORX screwdriver, to remove screws connecting the probe cables and screws connecting the back panel.

To remove the module

CAUTION: Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

1 Remove power from the instrument.

a Exit all logic analysis sessions. In the session manager, select Shutdown.

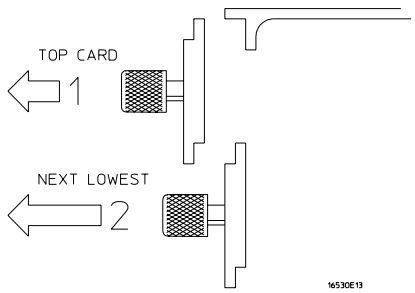
b At the query, select Power Down.

c When the “OK to power down” message appears, turn the instrument off.

d Disconnect the power cord.

2 Loosen the thumb screws.

Starting from the top, loosen the thumb screws on the filler panels and cards located above the module and the thumb screws of the module.



3 Starting from the top, pull the cards and filler panels located above the module half-way out.

4 If the module consists of a single card, pull the card completely out.

If the module consists of multiple cards, pull all cards completely out.

5 Push all other cards into the card cage, but not completely in.

This is to get them out of the way for removing and replacing the module.

6 If the module consist of a single card, replace the faulty card.

If the module consists of multiple cards, remove the cables from J9 and J10 of all cards. Remove the 2x10 cables from J4, J5, J7, and J8 from the master card. Remove the faulty card from the module.

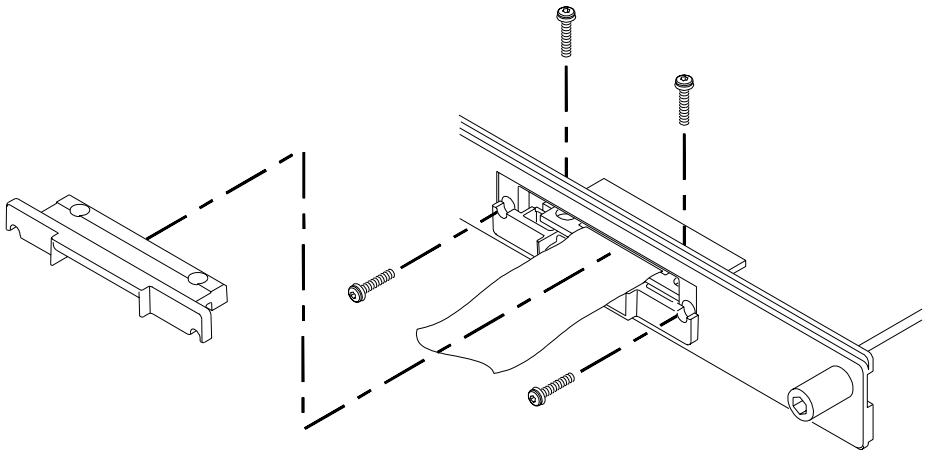
To remove the logic analyzer cable

1 Remove power from the instrument

- **a** Exit all logic analysis session. In the session manager, select Shutdown.
- **b** At the query, select Power Down.
- **c** When the "OK to power down" message appears, turn the instrument off.
- **d** Disconnect the power cord.

2 Remove the logic analyzer cable clamp.

- **a** Remove two screws that secure the top logic analyzer cable clamp to the outside rear panel.
- **b** Remove two screws that secure the top cable clamp to the inside rear panel.
- **c** Slide the top cable clamp out of the rear panel.



16760e18

3 Remove the logic analyzer cable.

- **a** Gently lift the logic analyzer cable end connector from the circuit board connector (J1 or J2).
- **b** Remove the logic analyzer cable end connector through the rear panel. The bottom cable clamp will also be removed with the logic analyzer cable.

4 If the logic analyzer cable is faulty, replace the cable and follow the next procedure to install the replacement logic analyzer cable.

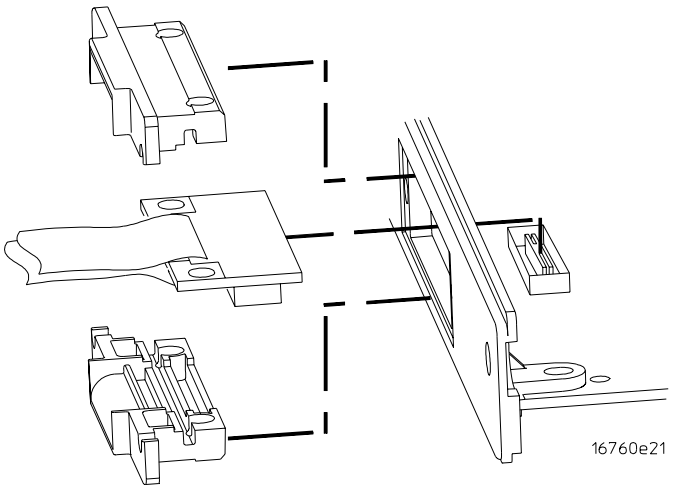
To install the logic analyzer cable

1 Connect the logic analyzer cable to the logic analyzer circuit board.

a Insert the logic analyzer cable to the logic analyzer circuit board.

b Align the logic analyzer cable end connector with the circuit board cable connector (J1 or J2) and gently apply pressure to seat the logic analyzer cable onto the circuit board connector.

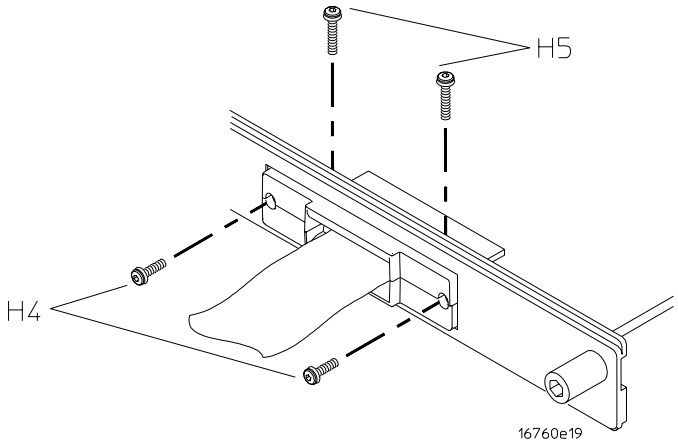
c Insert the top and bottom logic analyzer cable clamps into the rear panel.



2 Secure the cable clamp to the rear panel.

a Install the two longer screws (H5) vertically through the top cable clamp into both the bottom cable clamp and the circuit board. Do not tighten the screws yet.

b Install the two shorter screws (H4) through the rear of both cable clamps into the rear panel. Do not tighten the screws yet.

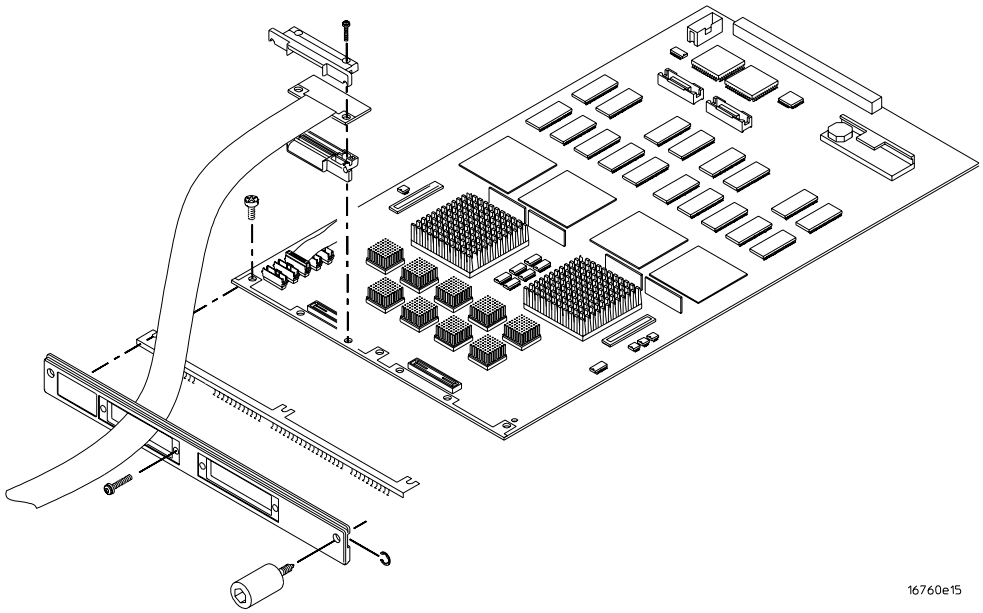


c Tighten the short rear panel cable clamp screws (H4) to 5 in/lb. Then tighten the longer cable clamp screws (H5) to 5 in/lb.

CAUTION: If you over tighten the screws, the threaded inserts on the rear panel, the threaded inserts on the circuit board, or the cable clamp itself might break. Tighten the screws only enough to hold the cable in place, approximately 5 in/lb.

To replace the circuit board

1. Remove both logic analyzer cables using the "To remove the logic analyzer cable" procedure on page 134.
2. Remove the four screws attaching the ground spring and back panel to the circuit board, then remove the back panel and the ground spring.
3. Replace the faulty circuit board with a new circuit board. On the faulty board, make sure the 20-pin ribbon cable is connected between J3 and J6.
4. Position the ground spring and back panel on the back edge of the replacement circuit board. Install four screws to connect the back panel and ground spring to the circuit board.
5. Install both logic analyzer cables using the procedure "To install the logic analyzer cable" on page 135.



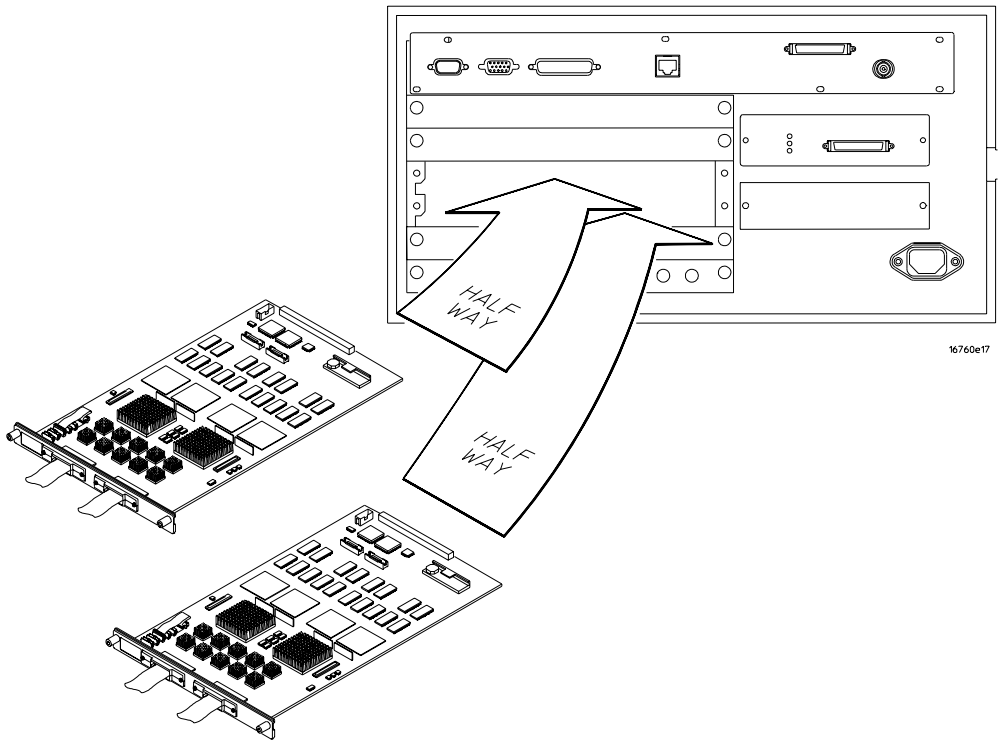
To replace the module

1 If the module consists of one card, go to step 2.

If the module consists of more than one card, connect the cables together in a master/expander configuration. Follow the procedure "To configure a multicard module" in chapter 2.

2 Slide the cards above the slots for the module about halfway out of the mainframe.

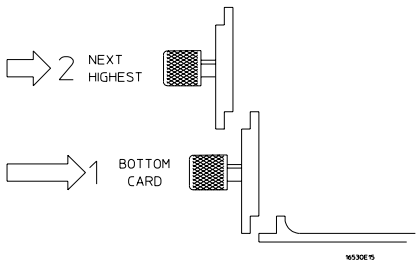
3 With the probe cables facing away from the instrument, slide the module approximately halfway into the mainframe.



4 Slide the complete module into the mainframe, but not completely in.

Each card in the instrument is firmly seated and tightened one at a time in step 6.

5 Position all cards and filler panels so that the endplates overlap.



6 Seat the cards and tighten the thumbscrews.

Starting with the bottom card, firmly seat the cards into the backplane connector of the mainframe. Keep applying pressure to the center of the card endplate while tightening the thumbscrews finger-tight. Repeat this for all cards and filler panels starting at the bottom and moving to the top.

CAUTION: Correct air circulation keeps the instrument from overheating. For correct air circulation, filler panels must be installed in all unused card slots. Keep any extra filler panels for future use.

To return assemblies

Before shipping the module to Agilent Technologies, contact your nearest Agilent Technologies Sales Office for additional details. Information on contacting Agilent can be found at http://www.agilent.com.

1 Write the following information on a tag and attach it to the module.

- Name and address of owner
- Model number
- Serial number
- Description of service required or failure indications

2 Remove accessories from the module.

Only return accessories to Agilent Technologies if they are associated with the failure symptoms.

3 Package the module.

You can use either the original shipping containers, or order materials from an Agilent Technologies sales office.

CAUTION: For protection against electrostatic discharge, package the module in electrostatic material.

4 Seal the shipping container securely, and mark it FRAGILE.

7

Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your module.

Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Agilent Technologies part number, indicate the quantity desired, and address the order to the nearest Agilent Technologies Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Agilent Technologies Sales Office.

Direct mail order system

To order using the direct mail order system, contact your nearest Agilent Technologies Sales Office.

Within the USA, Agilent Technologies can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the Agilent Technologies Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Agilent Technologies Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and no invoices.

In order for Agilent Technologies to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Agilent Technologies Sales Office. Addresses and telephone numbers are located in a separate document shipped with the *Agilent Technologies 16700-Series Logic Analysis System Service Manual*.

Exchange assemblies

Some assemblies are part of an exchange program with Agilent Technologies.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Agilent Technologies.

After you receive the exchange assembly, return the defective assembly to Agilent Technologies. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Agilent Technologies will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest

Agilent Technologies Sales Office for information.

See Also "To return assemblies" on page 140.

Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

Information included for each part on the list consists of the following:

- Reference designator
- Agilent Technologies part number
- Total quantity included with the module (Qty)
- Description of the part

Reference designators used in the parts list are as follows:

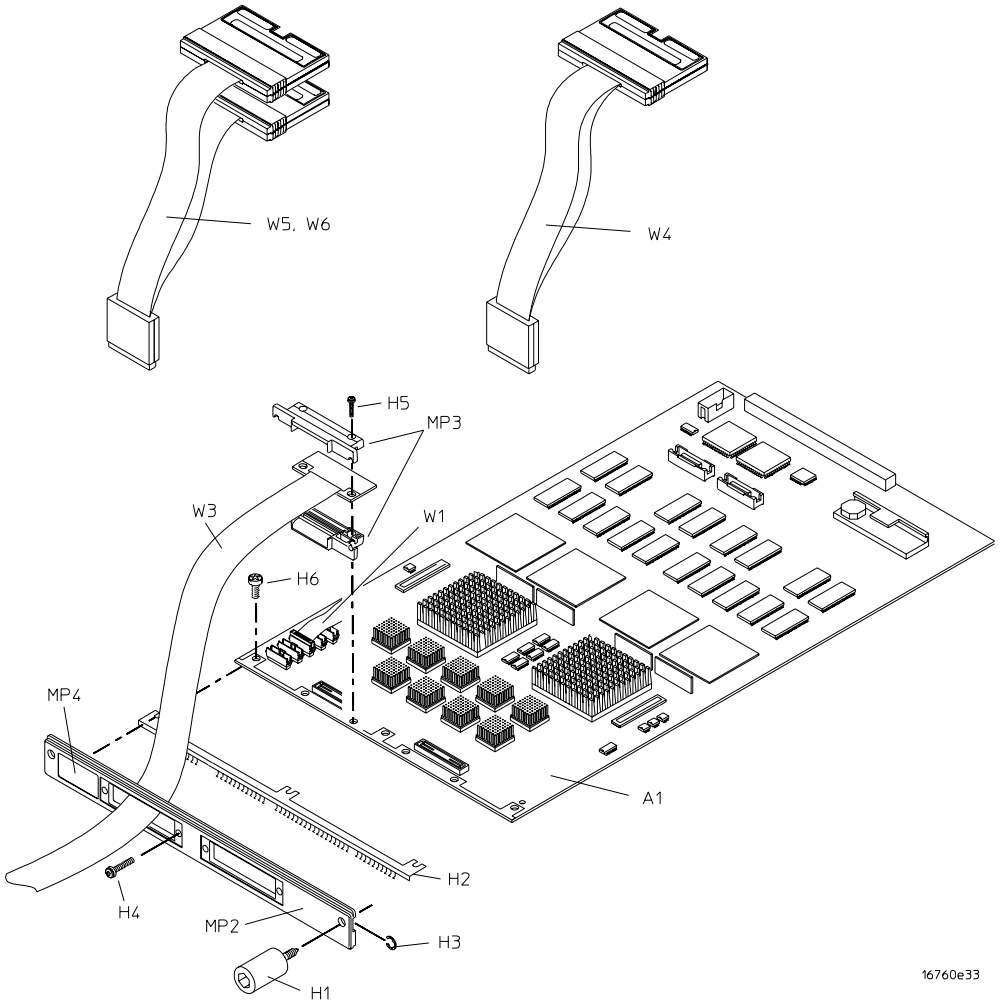
- A Assembly
- H Hardware
- J Connector
- MP Mechanical Part
- W Cable

Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
Exchange Assemblies			
	16760-69516		Exchange Acquisition Board Assembly
Replacement Assemblies			
A1	16760-66516	1	Acquisition Board Assembly
A2	16760-60001	0	Stimulus Board Assembly
H1	16500-22401	2	Panel Screw
H2	16500-29101	1	Ground Spring
H3	0510-0684	2	Retaining Ring
H4	0515-0372	4	M3.0x0.5 8mm T10 (Cable Clamp to Rear Panel)
H5	0515-0375	4	M3.0x0.5 16mm T10 (Cable Clamp to Acquisition Board)
H6	0515-0430	3	MSPH M3.0x0.50 6mm T10 (Rear Panel to Acquisition Board)
MP1	01650-94312	1	Label - Probe and Cable
MP2	16760-44107	1	Rear Panel
MP3	16760-44108	4	Logic Analyzer Cable Clamp (two clamps per cable)
MP4	16760-94309	1	ID Label
MP5	7121-0850	1	Label - Antistatic
W1	16555-61605	1	Cable (2x10)
W2	16715-60001	1	Master/Expander Cable Kit
W3	16760-61601	1	Logic Analyzer Cable
W4	16760-61602	1	Differential Probe (E5379A)
W5	16760-61603	1	Single-Ended Probe (E5378A)
W6	E5380-61601	1	Cable (E5380A)
Accessories for Connectivity to the System Under Test			
	1253-3620		Samtec Connector
	16760-02302		Shroud for 0.062" PC Boards
	16760-02303		Shroud for 0.120" PC Boards
	16760-68702		*Shroud/Connector Kit for 0.062" PC Boards
	16760-68703		*Shroud/Connector Kit for 0.120" PC Boards
	1252-7431		MICTOR Connector
	E5346-44703		MICTOR Shroud for 0.170" PC Boards
	E5346-44704		MICTOR Shroud for 0.125" PC Boards
	E5346-68700		*Shroud/Connector Kit for 0.125" PC Boards

*Shroud/Connector kits include connectors (Qty 5) and shrouds (Qty 5) for the indicated system under test circuit board thickness.

Exploded View



Exploded view of the 16760A logic analyzer

8

Theory of Operation

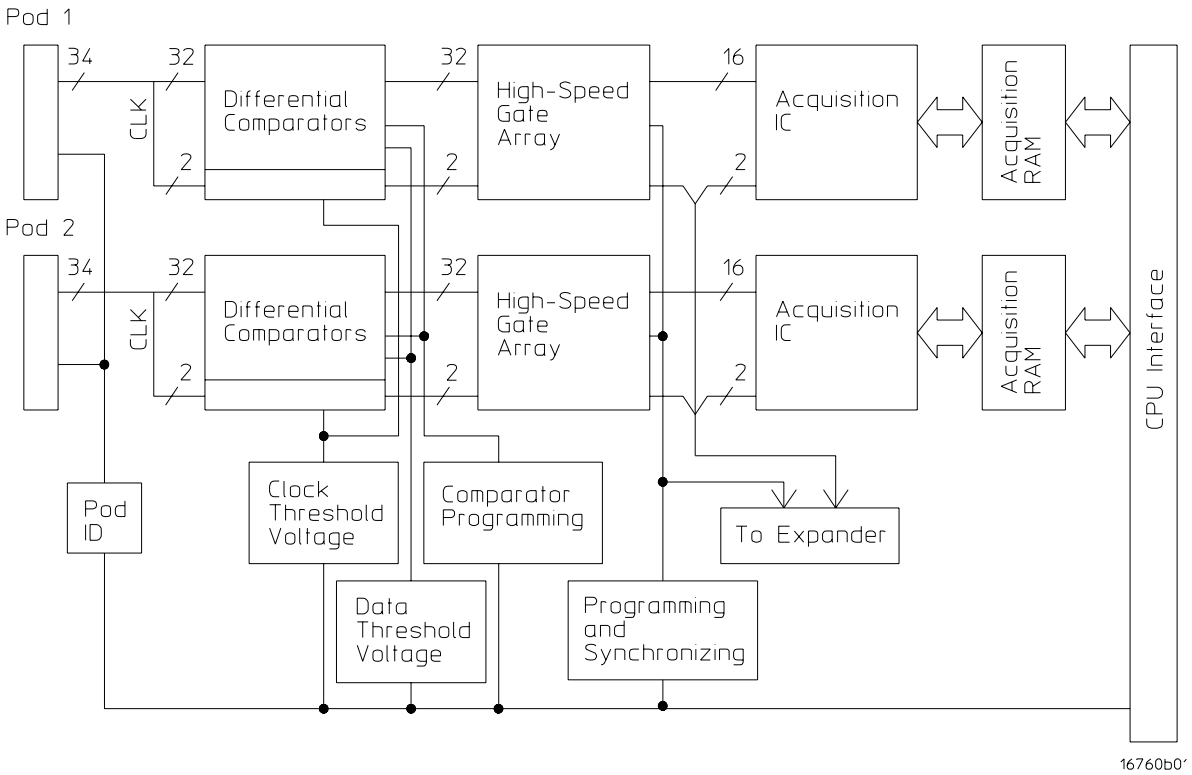
This chapter presents the theory of operation for the logic analyzer module and describes the self-tests.

The information in this chapter is to help you understand how the module operates and what the self-tests are testing. This information is not intended for component-level repair.

Block-Level Theory

The block-level theory of operation is divided into two parts: theory for the logic analyzer used as a single-card module or as a master card in a multi-card module, and theory for the logic analyzer used as an expander card in a multi-card module. A block diagram is shown before each theory.

The 16760A logic analyzer



Probe Adapter and Pods. Each pod includes 17 differential channels of analysis data, a threshold voltage input, two serial I2C lines for adapter probe identification, and 50 ground signals. The 17 differential channels of are fed from the probe adapter into the logic analyzer cable (pod) input. For signal-ended operation, the negative side of each of the 17 differential signals is coupled to ground inside the single-ended probe adapter.

On the end of the Samtec probe adapter is a 100-pin application-specific Samtec

connector. The mate to this Samtec connector must be designed into and installed in the system under test. Analysis of single-ended or differential signals is performed depending on whether the single-ended or differential probe adapter is used.

A Mictor-compatible probe adapter is also available. Like the Samtec probe adapter, the Mictor probe adapter is used for single-ended signal analysis through a Mictor connector designed in and installed into a system under test. Note that the performance of the logic analyzer module is limited when a Mictor-compatible probe adapter is used.

A threshold voltage input is provided through the probe adapter and pod for the user to configure the logic analyzer threshold voltage using the threshold voltage of the system under test. The logic analyzer module will then utilize the threshold voltage input to determine the logic high and logic low state of the incoming signals. The logic analysis system user interface allows the user to select the threshold voltage input. The threshold voltage input is designed with safeguards to protect the logic analyzer module from destructive effect of electro-static discharge (ESD).

The serial I2C lines are used to communicate with the probe adapter for identification. Periodic polling allows hot insertion of the probe adapter to the 16760A pod. When the probe adapter is installed at the end of the pod, the logic analyzer module polls the ID of the probe adapter. The module then configures itself for either single-ended or differential signal analyzer. The serial I2C lines are also designed with ESD safeguards.

The pods provide a 5 Vdc $\pm$5% auxiliary power to the end of the cable. A thermal protection circuit senses any over-current and automatically disables the auxiliary power. The auxiliary power circuit is designed wit safeguards to protect the logic analyzer module from the effects of electro-mechanical interference (EMI). Diatonically, a voltage ramp circuit allows an analysis probe to be hot inserted onto the end of the pod cable. Note that there are currently no analysis probes or other accessories utilizing this auxiliary power that are designed for the 16760A logic analyzer module as of the printing of this service manual.

Comparators. The comparators are differential input/differential output devices that interpret the incoming data and clock signals as either high or low. Threshold voltage, programmed by the user through the user interface, is set by a digital-to-analog converter (DAC) coupled to the negative side of the differential signal through a precision resistor. There are separate DAC-driven threshold voltages for the data and for the clock. In addition, the comparator contains a diode in which the junction temperature is monitored to ensure the module is being properly cooled.

Much of the performance optimization for the module is accomplished by the comparators, including channel delay setting (EyeFinder), programming of input resistance, and frequency compensation adjustment. Module operation such as

state clock modes and configuration are also done by the comparators. A digital-to-analog convertor (DAC) provides the module threshold voltage for single-ended operation. The voltage at the DAC outputs are buffered to prove sufficient line drive. An analog switch is used to channel either the module threshold voltage from the DAC or the threshold voltage input from the system under test to the comparators.

High Speed Gate Array. The high speed gate arrays sample the incoming data in the high speed state modes. The gate arrays have differential inputs and single-ended outputs and translate the incoming data from differential to single-ended signals. The output of the high speed gate arrays is channeled to the input of the acquisition ICs. A synchronizing signal ensures the gate arrays sample the data in step. A programming interface configures the operation of the gate arrays. In addition, each gate array device contains a diode in which the junction temperature is monitored to ensure the module is being cooled properly.

Acquisition IC. Each acquisition circuit is made up of a single acquisition IC. Each acquisition IC functions as a 17-channel state/timing logic analyzer. Two acquisition ICs are included on every single logic analyzer card for a total of 32 data channels and 2 clock/data channels. All of the sequencing, storage qualification, pattern/range recognition and even counting functions are performed by the acquisition IC.

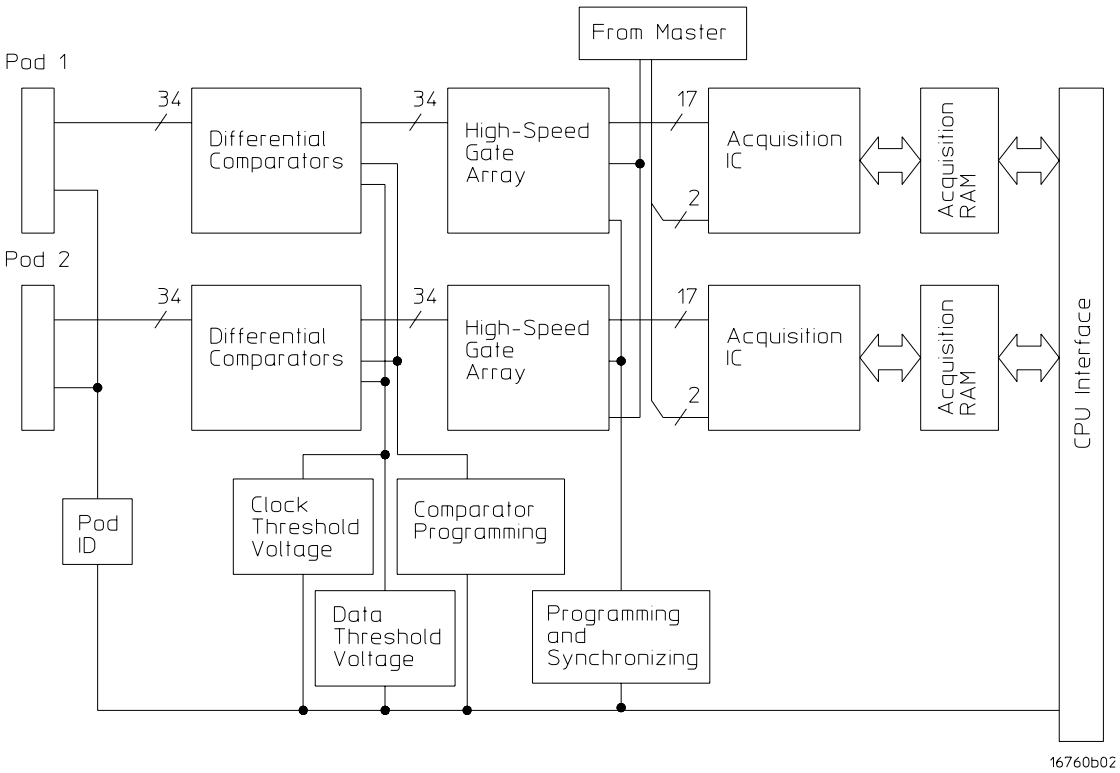
The acquisition ICs perform master clocking functions. The state acquisition clock is sent to each acquisition IC, and the acquisition ICs generate their own sample clock. Every time the user selects RUN, the acquisition ICs individually perform a clock optimization before data is stored. Clock optimization involves using programmable delays in the acquisition ICs to position the master sampling clock transition where valid data is captured. This procedure reduces the effects of channel-to-channel skew and other propagation delays.

In timing acquisition mode, a 100 MHz backplane clock from the logic analysis system mainframe drives the sample rate of the acquisition ICs. A master acquisition IC monitors the RUN signal asserted based on user input. The master acquisition IC then gates the sample clocks to all other acquisition ICs in the module.

Acquisition memory. The acquisition memory is a bank of 16-bit SDRAM devices and stores the processed data from the acquisition IC. Acquisition memory input/output is controlled by a memory controller, a bank of field programmable gate arrays (FPGA). The memory controller is initialized when power is applied to the logic analysis system from files stored on the system hard disk drive. During normal operation of the module, then memory controller is reprogrammed based on configuration of the module from user input. a second initialization file is loaded into the memory controller when the performance verification software is loaded into the system.

CPU Interface. The CPU interface is a programmable logic device that converts the bus signals generated by the microprocessor on the mainframe CPU card into control signals for the logic analyzer module. All functions of the state and timing module can be controlled from the backplane of the mainframe system including storage qualification, sequencing, assigning clock edges, RUN and STOP, and thresholds. Data transfer between the logic analyzer cards and the mainframe CPU is also accomplished through the CPU interface.

Master/Expander Configuration



Connectors J3 and J8 route clock and signals for operational accuracy calibration to expander boards in a master/expander multicard module. The master-configured module has the common connector (J3) cabled to the master connector (J6) expander board have their common connector cabled to the expander connectors (J4, J5, J7, and J8) of the master-configured board. Clock signals generated from either the master acquisition IC (timing mode) or from the system under test (state mode) are distributed to the expander boards through the master/expander star connectors. Clock generation is disabled to all expander boards. Additionally, a pattern found signal is routed from all configured expander boards to the master board through the star connectors. When the module is in pattern search mode, the pattern found signal is asserted by the expander board with the found pattern.

Connectors J9, J10, J500, and J501 form and acquisition IC pattern resource bus.

In addition to the master board, identification and operational configuration of the expander boards are done through the CPU interface.

Self-Tests Description

The self-tests for the logic analyzer identify the correct operation of major functional areas in the module.

CPLD Register Test. The CPLD Register Test verifies that the 16700-series backplane can communicate with the 16760A module CPLD. The CPLD is used to configure the backplane and the memory devices. The test is done using both a walking “1” and walking “0” pattern. After the pattern has been stepped, internal device registers are read.

Passing the CPLD Registers Test implies that the module backplane device can be properly configured for module setup and data download.

Load FPGA Test. The Load FPGA Test verifies that the backplane interface device and the data memory control device can be configured. Configuration data is read from a file. During the configuration process, status signals are checked to verify the 16760A module hardware is operating properly during the configuration upload.

Passing the Load FPGA Test implies that the module can be properly configured for normal operation.

FPGA Register Test. The FPGA Register Test verifies that the read/write registers of the backplane interface device and the memory control device can be written to then read. Both a walking “1” and “0” pattern is written to the device registers. The registers are then read and compared with known values.

Passing the FPGA Registers Test implies that the module hardware configuration can be properly managed as part of normal module operation.

Memory Data Bus Test. The Memory Data Bus Test verifies the read/write access of the acquisition module from the system backplane. In addition, some of the operations of the acquisition memory and control are also tested. A walking “1” and “0” is written to the first memory location. The contents of the first memory location is then downloaded and compared with known values.

Passing the Memory Data Bus Test implies that data stored in the acquisition memory can be uploaded from the 16760A module to the 16700-series system.

Memory Address Bus Test. The Memory Address Bus Test verifies the operation of the acquisition memory address bus. After initializing the acquisition memory, the address bus is exercised with a walking “1” and “0” pattern. At each

resulting memory address, test data is stored. The test data is then downloaded and compared with known values.

Passing the Memory Address Bus Test implies that each signal line of the acquisition memory address bus is operational, and therefore all locations in the acquisition memory can be accessed.

HW Assisted Memory Cell Test. After verifying the acquisition memory address bus signal lines using the Memory Address Bus Test, the HW Assisted Memory Cell Test does a read/write test on every location in the acquisition memory. Each location in acquisition memory is filled with a test data pattern. After loading acquisition memory, the test data at each memory location is downloaded then compared with known values.

Passing the HW Assisted Memory Cell Test implies that each location in acquisition memory can be accessed, written, read, and can properly store data.

Memory Unload Modes Test. The Memory Unload Modes Test verifies the CPU interface can properly manage the acquisition memory unload in both full-channel, half-channel, and interleaved modes. Test data is written to acquisition memory. Different unload modes are selected, then the data is read and compared with known values.

Passing the Memory Unload Modes Test implies that the data can be reliably read from acquisition memory in full-channel, half-channel, or interleaved mode. This test along with the Memory Data Bus Test and Memory Address Bus Test provide complete testing of acquisition memory downloading through the CPU interface.

Memory DMA Unload Test. The Memory DMA Unload Test performs the same functions as the Memory Unload Test, except DMA backplane transfers are used to read the data from acquisition memory.

Memory Sleep Mode Test. The Memory Sleep Mode Test verifies the self refresh mode of acquisition memory devices. Memory self refresh mode is enabled when the memory control device is reprogrammed during normal operation.

Passing the Memory Sleep Mode Test verifies the acquisition memory will retain data during changes in 16760A operating modes during normal operation.

HW Accelerated Search Test. The HW Accelerated Search Test verifies the fundamental search capabilities of the module. Acquisition RAM is loaded with test data, and the search registers in the gate arrays are programmed with test patterns. Basic search functions including return and count pattern, are done and monitored for success.

Passing the HW Accelerated Search Test implies that the module's fundamental Hardware accelerated pattern search capabilities are operating and that pattern searches and pattern occurrence counts can be performed.

Chip Registers Read/Write Test. The Chip Registers Read/Write Test verifies that the registers of each acquisition IC are operating properly. Test patterns are written to each register on each acquisition IC, read, and compared with known values. The registers are reset, and verified that each register has been initialized. Test patterns are then written to ensure the chip address lines are not shorted or opened. Finally test data is written to registers of individual acquisition ICs to ensure each acquisition IC can be selected independently.

Passing the Chip Registers Read/Write Test implies that the acquisition IC registers can store acquisition control data to properly manage the operating of each IC.

Analyzer Chip Memory Bus Test. The Analyzer Chip Memory Bus Test verifies the operation of the acquisition memory buses between acquisition ICs. After initializing the memory a walking "1" and "0" pattern is created at the output of the acquisition ICs. This test data is stored in memory, read, and compared with known values.

Passing the Analyzer Chip Memory Bus Test implies that the acquisition memory buses between the acquisition ICs and acquisition memory is operating, and that acquisition data can propagate from the ICs to memory.

System Clocks (Master/Slave/Psync) Test. The System Clocks (Master/Slave/Psync) Test verifies the system clock are functional between all boards in a master/expander multi-card module. The module is configured for a simple measurement and test data is created. The test data is then downloaded and compared with known values.

Passing the System Clocks (Master/Slave/Psync) Test implies that the acquisition ICs of each expander board of a multi-card configuration can properly receive system clocks, and that all acquisition ICs in the multi-card module will properly capture data.

Analyzer Memory Bus SU/H Measure. The Analyzer Memory Bus SU/H Measure is an internal test that ensures the timing between the acquisition IC and acquisition memory is within acceptable parameters.

System Backplane Clock Test. The System Backplane Clock Test verifies the 100 MHz acquisition system clock. The test also ensures an on-board phase-locked loop can properly generate multiples of the acquisition system clock frequency. The 100 MHz acquisition system clock is first routed directly to the acquisition ICs. A timer is initialized, run, and stopped after 100ms. the counter is read, and compared with a known value. The acquisition system clock is then routed to the phase-locked loop to generate a frequency of 166.7 MHz. Again, the counter is initialized, run, and stopped after 100ms. The counter is read, and compared with a known value.

Passing the System Backplane Clock Test implies that the system acquisition clock is operating, and is within 5% of the desired acquisition frequency. Note

that the procedure to test the Time Interval Accuracy in Chapter 3 provides a more reliable characterization of clock oscillator drift.

Inter-chip Resource Bus Test. The Inter-chip Resource Bus Test verifies the resource lines that run between each acquisition IC to ensure that the resource lines can be both driven as outputs and read as inputs. The resource registers are written with test patterns, read back, then compared with known values. The resource registers are then written with test patterns, read back from a different acquisition IC, and then compared with known values.

Inter-module Flag Bits Test. Flag bits are used for module-to-module communication within the 16700-series system. The Inter-module Flag Bits Test verifies that the flag bit lines can be driven and received by each acquisition IC in each module. Test patterns are written to the flag registers, read by the other acquisition ICs in the other modules, and then compared with known values.

Passing the Inter-module Flag Bits Test implies that the acquisition ICs can communicate using Flag Bits through the CPU interface and the 16700-series backplane, and that the operations utilizing the flag bits can be properly recognized by all modules in the system.

Global and Local Arm Lines Test. The Global and Local Arm Lines Test verifies that the local arm signal can be received by each acquisition IC on the master board. The test also verifies the global arm signal can be driven by each acquisition IC on a master board, and received by all acquisition ICs in the module on the master and on all expander boards. The arm lines are asserted and read at the acquisition ICs to ensure each acquisition IC recognizes the signal.

Passing the Global and Local Arm Lines Test implies any acquisition ICs on the master board can arm the module, and that all acquisition ICs can recognize the arm signal.

EEPROM Test. The EEPROM Test verifies the operation of the module EEPROM, which stores the operational accuracy calibration factors. The existing contents of the EEPROM are uploaded into system memory. The EEPROM is overwritten with test patterns to verify that each cell in the EEPROM can independently store a 1 or 0. After the test has completed the original contents of the EEPROM are restored and its checksum verified.

Passing the EEPROM Test implies that the current operational accuracy calibration factors can be stored and then retrieved for use by the module to optimize its performance.

ADC Test. The ADC Test verifies the operation on the module analog-to-digital convertor (ADC) used in the module operational accuracy calibration, probe adapter identification, and on-board temperature monitoring. The ADC has built-in test voltage channels which monitors three test voltages. The output of the channels is then compared with known values.

Passing the ADC Test implies that the analog-to-digital convertor is operating properly and that the data paths around the ADC can properly pass data.

Probe ID Read Test. The Probe ID Read Test verifies that the analog-to-digital convertor (ADC) tested above and the on-board digital-to-analog convertor are operating to read the probe adapter ID. Probe adapter identification is done using a precision resistor. When the probe adapter is installed onto the probe cable, the precision resistor completes a voltage divider network. The Probe ID Read Test exercises the voltage divider network and then reads the voltage across the precision resistor and compares the voltage to know values.

Passing the Probe ID Read Test implies that any of the compatible probe adapters can be properly identified, causing the module to configure itself correctly.

Demux Data Arrays Programming Test. The Demux Data Arrays Programming Test verifies that the gate arrays' programming bits can be properly configured. Various test patterns are written to the programming port of the gate arrays, then read back and compared to expected values.

Passing the Demux Data Arrays Programming Test implied that the gate arrays can be programmed according to the operating mode of the module.

Comparators Programming Test. The Comparators Programming Test verifies that the comparators' programming bits can be properly configured. Various test patterns are written to the programming port of each comparator, then read back and compared to expected values.

Passing the Comparators Programming Test implies that the comparators can be programmed according to the operating mode of the module.

Data Path Pass-Thru Test. The Data Path Pass-Thru Test ensures that incoming data can flow correctly between the comparators and the acquisition ICs. The gate arrays are programmed for low-speed acquisition, which makes them invisible to data. The comparators are configured in test mode to drive a toggling signal on one of the comparator outputs while all other outputs are held quiet. The activity detectors in the acquisition ICs are monitored to verify that only the expected signal is toggling. The test is repeated for each comparator output.

Passing the Data Path Pass-Thru Test implies that incoming data can flow from the module front end to the acquisition ICs without errors for low speed acquisition modes (Timing, 200 MHz State, and 400 MHz State acquisition modes).

Data Path Demux Test. The Data Path Demux Test operates the same as the Data Path Pass-Thru Test, except the gate arrays are programmed for high-speed acquisition where the incoming data is demultiplexed to improve throughout.

Passing the Data Path Demux Test implies that incoming data can flow from the module front end to the acquisition ICs without errors for high speed acquisition modes (800 MHz State and 1250 Mb/s State acquisition modes).

Comparators V Offset Test. The Comparators V Offset Test completes the operation check of the comparators. Voltage offset is programmed into the comparators to ensure proper signal symmetry of the differential signal with respect to a threshold. The test verifies that the voltage offset can be programmed at all points throughout the offset range.

Passing the Comparators V Offset Test implies that the comparator voltage offset is programmable to ensure differential data signals are properly captured.

Comparators Calibration Test. The Comparators Calibration Test runs the comparator calibration to optimize the performance of the module. Both analog and digital domain tests are run to optimize signal integrity in the module front end.

Passing the Comparators Calibration Test implies that the comparators are completely operational and can be performance optimized. Note that the resulting calibration factors are not stored.

LA Chip Calibration Test. The LA Chip Calibration Test ensures that each acquisition IC in the module can perform an operational accuracy self-calibration every time Run is selected. The module is set in various configurations, after which the self-calibration routing is initiated. The results of the self-calibration is then checked to see if self-calibration was successful.

Passing the LA Chip Calibration Test implies that the module can reliably perform an operation accuracy self-calibration every time Run is selected. Consequently the incoming data is optimized to reduce channel-to-channel skew so the acquisition ICs can reliably capture the incoming data.

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About this edition

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New editions are complete revisions of the manual. Many product updates do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.